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Exploring Performance of Nanoscale Reconfigurable Germanium Transistor for Advanced Logic Gate Design and Functionality

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ABSTRACT: This paper investigates the electrical characteristics of a germanium reconfigurable transistor and comprehensively evaluates the impact of crucial design parameters on the device performance. The transistor can operate in both n-mode and p-mode simply by adjusting the bias of the electrodes. The findings demonstrate that the on-state current for n-mode operation is 1.3×10^{-4} (A/µm) and for p-mode operation is 8.5×10^{-5} (A/µm). Additionally, the on/off current ratio is 1.34×10^{5} for n-mode and 2.35×10^{5} for p-mode. The subthreshold swing of the device has also been computed. In n-mode operation, a subthreshold swing of 95 mV/dec is achieved, while in p-mode, a subthreshold swing of 108 mV/dec is observed at the maximum slope of the transfer characteristics. A notable feature of this device is the incorporation of a two-input XNOR logic gate as well as a two-input AND logic gate within a single transistor. The implementation of logic gates using a single reconfigurable transistor presents significant benefits in terms of energy efficiency and speed for upcoming advanced integrated circuits.

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1- Introduction

Nowadays, the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) serves as the fundamental component of integrated circuits. The occurrence of short channel effects in the nanoscale regime necessitates a complex fabrication process to address this issue [1-3]. Consequently, the design of integrated circuits incorporating both n-type and p-type MOSFETs becomes challenging. The Reconfigurable Field Effect Transistor (RFET) emerges as a promising alternative to the traditional MOSFET [4-7]. A notable advantage of reconfigurable transistors is their Schottky source-drain architecture, featuring two gates - a control gate and a program gate capable of switching between n-mode and p-mode operations through a simple adjustment of the electrode bias. The control gate controls the device's on and off state, whereas the program gate adjusts the band bending at the drain side to enable the device to function in either n-mode or p-mode. This feature distinguishes them from conventional MOSFETs, which require a complex fabrication process to achieve n-type and p-type functionalities separately. Experimental investigations have been conducted on the operation of RFET, exploring the performance of nanowire RFET with silicon as the channel material. A three-gate RFET has been developed utilizing silicon as the channel material to regulate the charge carriers within the channel. This device is comprised of two program gates situated at the source and drain regions, with the control gate positioned in the center of the channel. By adjusting the gate voltages, the threshold voltage of the device can be controlled [8]. The U-shaped RFET, a three-dimensional device, exhibits enhanced drain current compared to traditional RFETs, with tunneling through the Schottky barrier serving as the primary current mechanism. Increasing the tunneling area is proposed as a solution to boost the drain current of the Silicon-based RFET [9]. An extended source RFET has also been introduced, where the source region is extended along the channel to increase the tunneling area [10, 11]. Furthermore, the impact of spacer length on the performance of Schottky source/drain RFETs has been studied, revealing that reducing the spacer length at the source side enhances the control gate electric field at the tunneling junction [12]. Additionally, a dual-doped source-drain configuration has been implemented to enable the transfer characteristics of an RFET without employing Schottky contacts in the device structure. However, it is worth noting that the fabrication process of this device poses challenges in the nanoscale regime [13-15]. The proposed device in [16] examines the influence of ferroelectric gate oxide on the functionality of a nanowire reconfigurable transistor featuring an arc-shaped source region. This device utilizes an extended Schottky contact across the channel region to enhance the tunneling area. The incorporation of ferroelectric gate oxide leads to a reduction in the subthreshold swing of the device, thereby enhancing its switching speed. A reconfigurable field

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effect transistor utilizing stacked nanosheets is a vertical device characterized by three parallel stacks. This design incorporates silicon as the channel material, with Schottky contacts utilized at both the source and drain junctions. The extended source region enhances the tunneling area, thereby resulting in an increase in the on-state current of the device [17]. In [18], a reconfigurable transistor utilizing an Al-Si-Al heterojunction in the form of a nanowire has been developed. The Schottky contacts are constructed using aluminum. This device successfully functions as a logic AND gate while demonstrating minimal variability between different devices. The proposed Al-Si Schottky contact provides a uniform barrier for both electrons and holes. A reconfigurable transistor utilizing a heterojunction of BN-MoS_2 has been developed with a side gate configuration. This device successfully performs three distinct functions: it operates as a diode, a double-side-gate reconfigurable logic transistor, and a top floating gate memory. Within this single double-side-gate device, reconfigurable logic operations such as OR and AND can be executed, achieving a current on/off ratio of approximately 10^4 [19]. A bipolar tunable reconfigurable transistor utilizing $MoTe_2/WSe_2$ has been developed as detailed in [20]. The modulation of the Fermi level and the corresponding Schottky barrier height is achieved through the gate voltage. In [21], a reconfigurable transistor utilizing two-dimensional $MoTe_2$ has been developed, which omits the control gate. In this configuration, the source and drain contacts are extended, effectively serving as the control gate. The variation in voltage between the source and drain contacts determines the primary carrier transport within the channel. The operational mechanism of the WSe_2 reconfigurable transistor has been demonstrated in [22]. This two-dimensional material configuration utilizes two programmable gates alongside a back gate for control. The modulation of the Schottky barrier height is facilitated by the programmable gates, resulting in an on/off current ratio of 10^6 in this device. A reconfigurable tunnel field effect transistor has been developed utilizing black phosphorus as the active material. This device is capable of functioning in both n-mode and p-mode configurations. The doping density required to initiate tunneling in both modes is regulated through the use of multiple gate structures [23]. An examination of reliability concerning temperature fluctuations on the functionality of reconfigurable transistors reveals that bias temperature instability leads to a degradation in the device threshold voltage [24]. The reconfigurable transistor has been utilized in biosensing applications. Biomolecules are situated within the cavity located between the gates. These biomolecules alter the surface potential and generate charges in the channel, which in turn affects the threshold voltage and subsequently the drain current [25, 26]. In a different application, a reconfigurable transistor is utilized as a pH sensor, wherein a cavity is embedded into the gate insulator. The threshold voltage of the device is altered in response to the pH level of the substance contained within the cavity [27].

The primary obstacle faced by RFET is the limited on-state current due to the elevated Schottky barrier height for both holes and electrons in silicon-based devices. This study comprehensively evaluates the electrical characteristics of a germanium-based Reconfigurable Field Effect Transistor (Ge-RFET) and examines the influence of critical design parameters on the device performance. Ge-RFET is characterized by its ability to offer a low identical Schottky barrier for both electrons and holes. Additionally, its low effective mass enhances the tunneling probability. Furthermore, a notable feature of the Ge-RFET is its ability to implement an XNOR and an AND two-input logic gate within a single device. The control gate plays a crucial role in determining the transistor's normal operating mode, including its threshold voltage and current flow. On the other hand, the program gate offers the flexibility to modify the transistor behavior for specific n-mode or p-mode operations, enabling it to perform a designated logic function. By configuring the control gate to establish a specific threshold voltage and the program gate to create a particular current path, the XNOR logic gate can be realized. When input signals are applied to the control and program gates, the transistor will exhibit behavior that implements the XNOR logic function through the output drain current. Furthermore, a single transistor is utilized to design a two-input AND logic gate by treating the control gate and drain electrode as the inputs and the drain current level as the output. This reconfigurability feature facilitates the implementation of complex digital circuits on a single device.

2- Device Structure and Simulation Set up

Fig. 1 presents the 2D schematics of the proposed Ge-RFET. This device consists of two gates, namely the control gate and the program gate. The control gate is responsible for the activation and deactivation of the device, while the program gate determines the operation mode (n-mode or p-mode) by creating the appropriate band bending at the drain side. In Fig.1 (b), the n-mode operation of the device is depicted, where the control gate bias (V_{CG}), program gate bias (V_{PG}), and drain bias (V_{DS}) are all positive. In this case, electrons accumulate in the channel, and the band bending at the drain side facilitates their transport towards the channel. Conversely, for p-mode operation, depicted in Fig.1 (c), all bias values are negative. When the control gate has a sufficiently negative value, holes accumulate in the channel, and the band bending at the drain side guides holes towards the drain electrode. The metal source and drain have been adjusted to have a work function of 4.34 eV, which enables the attainment of a Schottky barrier height of 0.34 eV for electrons and 0.43 eV for holes [28]. As a result, the transfer characteristics for both n-mode and p-mode operation exhibit a high degree of symmetry.

To ensure accurate evaluation of the device performance, numerical computations are conducted using the Silvaco device simulator [29], and following models are considered in the simulation: Thermionic emission model is activated which occurs when carriers possess energy levels exceeding the Schottky barrier, allowing them to overflow it; Direct tunneling involves carriers tunneling through the space charge

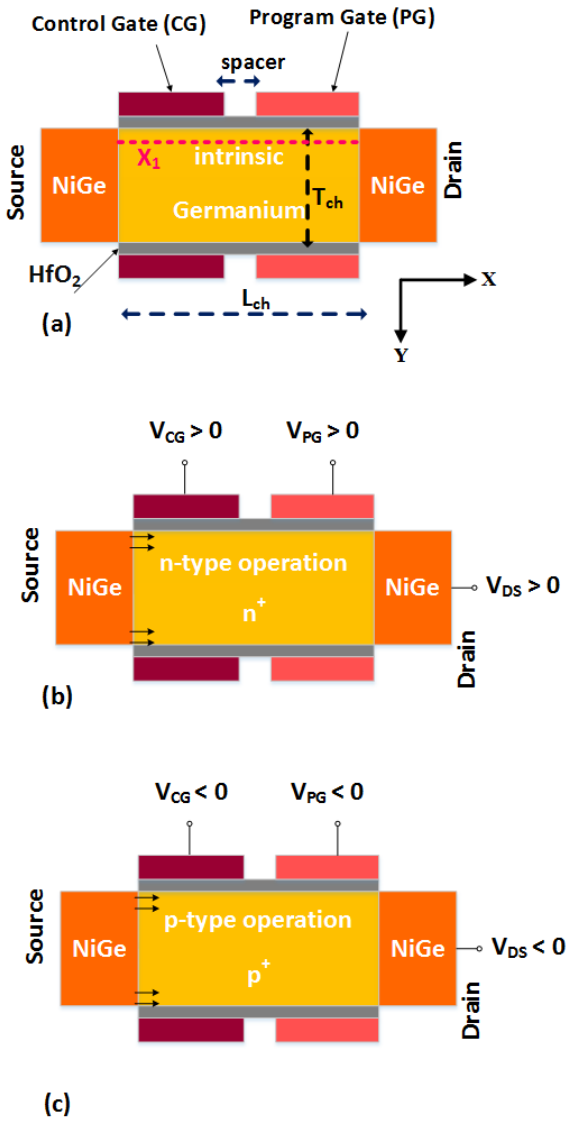

Fig. 1. (a) 2D schematic of the proposed Ge-RFET, the dashed line "X1" shows the direction in which the energy band diagram and carrier density are calculated. (b) n-mode operation and (c) p-mode operation of the proposed Ge-RFET.

region located at the junction of the source and channel region; Mobility models take into account carrier scattering effects, as well as the impact of horizontal and vertical electric fields on carrier mobility; Generation and recombination models analyze carrier density in the context of defects and traps. The initial design parameters are presented in Table 1.

3- Results and Discussions

The primary characteristic of Ge-RFET is its ability to operate in both n-mode and p-mode by simply adjusting the bias of the electrodes. The device utilizes a Schottky contact at the source and drain regions, leading to current transport based on Schottky current contact. The energy band diagram of the proposed Ge-RFET in the off-state and on-state for n-mode and p-mode operation is illustrated in Fig.2. In the case of n-mode operation (Fig. 2(a)) in the off-state (V_{CG}=0V, V_{PG}=1V, V_{DS}=1V), the Schottky barrier width at the interface of the source and channel region is significantly large. Consequently, the tunneling probability is very low. Under these conditions, carriers with higher energy than the Schottky barrier height surpass the barrier and undergo thermionic emission. The positive program gate bias induces band bending at the drain side, facilitating the flow of electrons. However, as the control gate bias increases (V_{CG}>0V, V_{PG}=1V, V_{DS}=1V), electrons accumulate in the channel, resulting in a thinner Schottky barrier width at the interface of the channel. This thin barrier enables direct tunneling, leading to a high on-state current. On the other hand, in the off-state condition of p-mode (Fig. 2(b)) (V_{CG}=0V, V_{PG}=-1V, V_{DS}=-1V), the hole density in the channel is very low, and the tunneling probability is also low. Consequently, only thermionic emission occurs. In the on-state (V_{CG}<0V, V_{PG}=-1V, V_{DS}=-1V), as the control gate bias increases towards more negative values, holes accumulate in the channel. This accumulation results in a thinner barrier width at the interface of the source and channel region, facilitating hole tunneling and an increase in drain current.

The carrier density distribution in the channel is shown in Fig.3 for both n-mode and p-mode operation during off-state and on-state conditions, along cut line 'X1'. In Fig. 3 (a), the electron density is illustrated along the device from the source to the drain, indicating the accumulation of electrons

Table 1. Initial design parameters of Ge-RFET.

Parameter	Value
Control/ Program Gate Length	12 nm
Gate Workfunction	4.35 eV
Gate Oxide thickness	1 nm-HfO_2
Channel Thickness (T_{ch})	10 nm
Channel Length (L_{ch})	41 nm
Spacer Length	10 nm

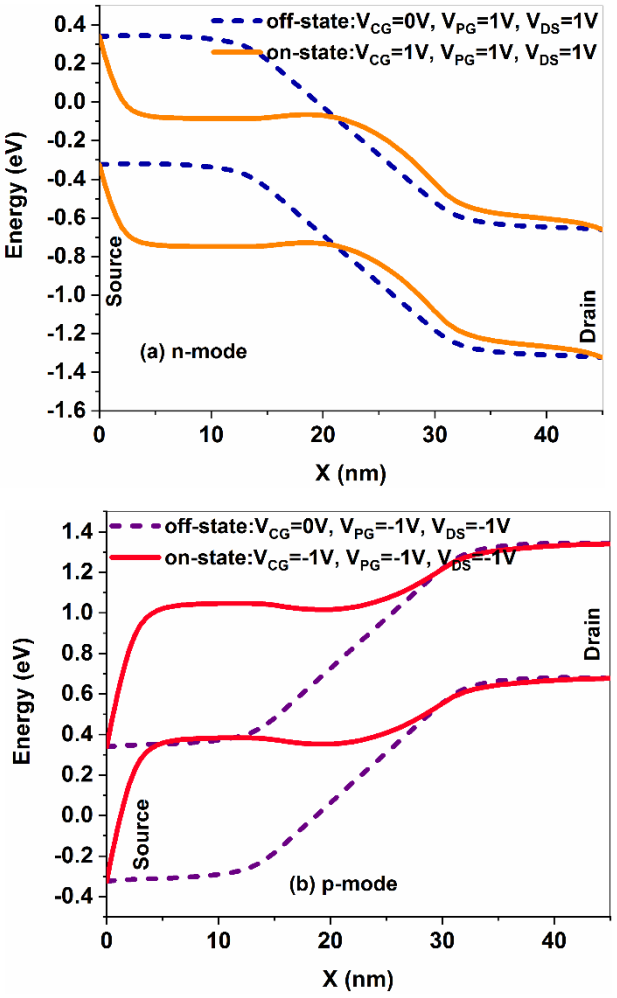

Fig. 2. Energy band diagram of the Ge-RFET in the off-state and on-state for (a) n-mode and (b) p-mode operation.

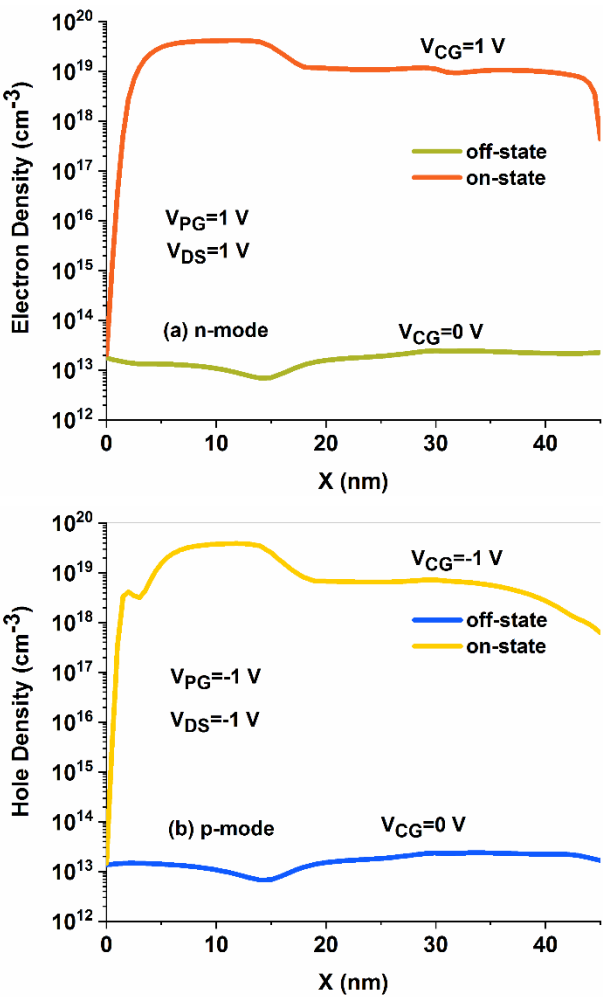

Fig. 3. Carrier density along the device from source to drain in the off-state and on-state for (a) n-mode and (b) p-mode operation.

in the channel when the control gate bias is at its maximum positive value. Conversely, for p-mode operation, as shown in Fig.3 (b), the accumulation of holes in the channel occurs when a negative bias is applied to the control gate.

Figure 4 depicts the transfer characteristics of the proposed Ge-RFET for both n-mode and p-mode operation. Remarkably, the device exhibits identical characteristics in both modes of operation. In the n-mode operation, where $V_{CG}>0$, $V_{PG}>0$, and $V_{DS}>0$, the control gate's positive value leads to the accumulation of electrons in the channel. Simultaneously, the positive value of the program gate induces appropriate band bending at the drain side, facilitating the flow of electrons from the source to the channel. Conversely, in the p-mode operation, where $V_{CG}<0$, $V_{PG}<0$, and $V_{DS}<0$, the negative value of the control gate causes the accumulation of holes in the channel. The program gate then modulates the band bending at the drain side, enabling the flow of holes along the channel. The results indicate that the on-state current for n-mode operation is 1.3×10^{-4} (A/μm) and for p-mode operation is 8.5×10^{-5} (A/μm). Moreover, the on/off current ratio is 1.34×10^{5} for n-mode and 2.35×10^{5} for p-mode. The subthreshold swing of the device, an indicator of its switching speed, has been computed. In n-mode operation, a subthreshold swing of 95 mV/dec is achieved, while in p-mode, a subthreshold swing of 108 mV/dec is observed at the maximum slope of the transfer characteristics. The constant current method is employed for calculating the drain current [30, 31]. In this approach, the current level has been chosen such that the transistor operates in the middle of the moderate inversion region. Basically, in the weak and moderate inversion regions, the high-electric field effects are reduced. By definition, threshold voltage (V_{th}) is the gate bias required for the drain to reach 10^{-7} (A/μm). The threshold voltage is 0.23 V for n-mode and -0.29 V for p-mode. The off-state currents in the n-mode and p-mode exhibit a minor difference. This effect is mainly attributed to the accumulation of charge within the channel. In intrinsic

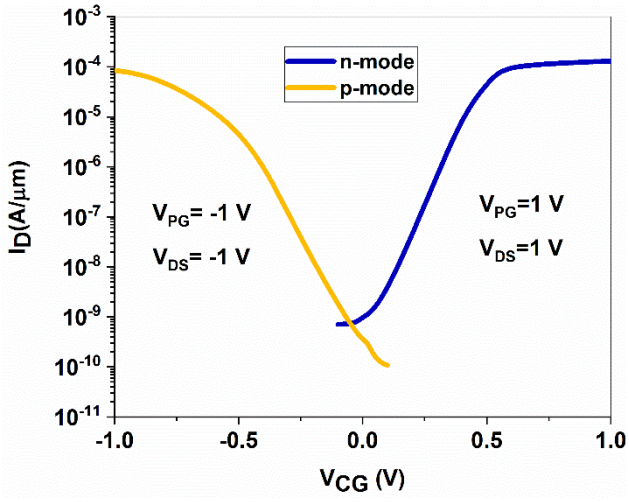

Fig. 4. Transfer characteristic of Ge-RFET for n-mode and p-mode operation.

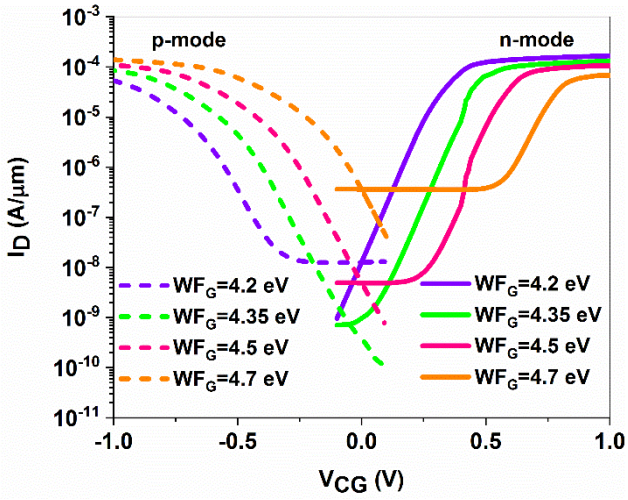

Fig. 6. ID-VCG curves of Ge-RFET as the work function value of the control gate and program gate is parametrized.

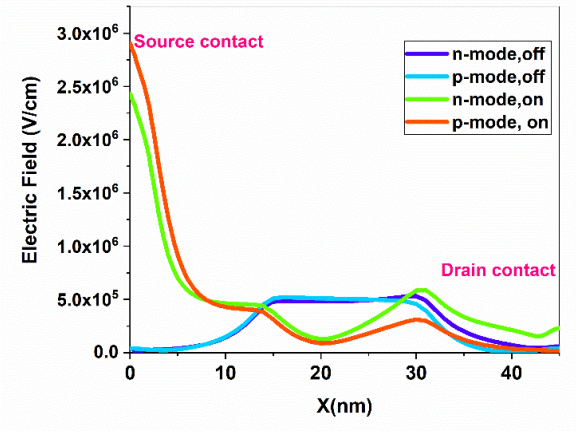

Fig. 5. Electric field along the device from source to drain in the off-state and on-state

germanium, one would expect an equal presence of electrons and holes, leading to no difference in the off-state current. However, the variation in work function between the gate material and the channel modifies the flat band condition in the off-state. Consequently, charge accumulation occurs in the channel, resulting in differing off-state currents for both n-mode and p-mode configurations. Implementing work function engineering alongside doping density variation in the channel can mitigate this effect.

The electric field distribution across the device from the source to the drain is depicted in both the off-state and on-state in Fig. 5. A notable characteristic of the Ge-RFET is that the program gate, which generates a vertical electric field, applies a voltage that diminishes the lateral electric field at the drain in the off-state. This configuration reduces the influence of drain bias on the generation of hot carrier effects and the gate tunneling current. Furthermore, the gate spacer provides additional separation between the drain region and the control gate area. Nevertheless, due to the thin gate oxide, it is reliable to utilize a thicker gate oxide with a higher dielectric constant to minimize the impact of scattering carriers tunneling through the gate oxide.

Figure 6 illustrates the impact of the work function of the control gate and program gate on the performance of the proposed Ge-RFET. The bias value of the control gate and the work function of the gate are in competition when it comes to modulating the channel charge density. It is crucial to have an optimal gate work function to achieve the same transfer characteristic for both n-mode and p-mode operations. During n-mode operation, increasing the gate work function towards 4.35eV leads to the depletion of the intrinsic channel region, resulting in a reduction of electron density in the channel. This, in turn, decreases the off-state current and increases the threshold voltage. However, a further increase in the gate work function causes the accumulation of holes in the channel, significantly increasing the off-state current. On the other hand, in p-mode operation, lower work function values lead to a high electron density in the channel. As the gate work function is increased towards 4.35 eV, electrons are depleted in the channel, leading to a decrease in the off-state current. Further increasing the gate work function results in an increase in hole density in the channel, consequently increasing the off-state current. Therefore, a work function of 4.35 eV is considered the optimal value for both n-mode and p-mode operations, as it achieves the minimum off-state current with an identical transfer characteristic.

Figure 7 depicts the impact of temperature on the performance of the Ge-RFET, specifically for n-mode and p-mode operation. It can be observed that the subthreshold

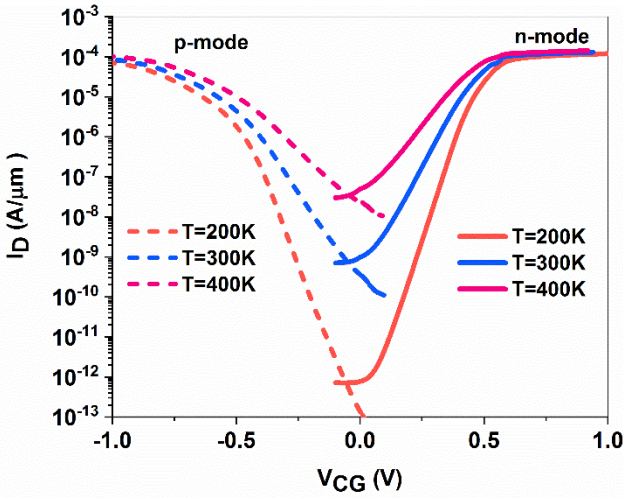

Fig. 7. Transfer characteristics of Ge-RFET as the temperature is varied for n-mode and p-mode operation.

characteristics and off-state current of the device are highly susceptible to temperature fluctuations. This phenomenon can primarily be attributed to the thermionic emission current originating from the source region. Basically, the subthreshold current increases as the thermal energy given to the charge carrier overcomes the work function of the metal source. Furthermore, as a result of the buildup of carriers caused by elevated thermionic emission, the threshold voltage of the device decreases with rising temperatures.

Temperature significantly influences carrier mobility. It is important to note that as temperature rises, mobility tends to decrease, primarily due to phonon scattering and dislocation scattering. Conversely, the relationship between doping density and temperature is direct, particularly at elevated doping densities; temperature variations have a minimal effect on mobility. Consequently, the relationship between mobility and temperature depends upon many parameters. Figure 8 depicts the effect of temperature on the carrier mobility of both electrons and holes in the on-state, illustrating that increased temperature correlates with reduced mobility.

The drain induced source tunneling (DIST) effect refers to the modulation of the space charge region at the interface of the source and channel interface by the drain electric field. This effect occurs in the absence of the gate bias. In the nanoscale regime, the DIST effect becomes a limiting phenomenon in Schottky transistors, leading to an increase in the off-state current and degradation of the subthreshold swing. Additionally, conventional Schottky transistors experience gate-induced drain leakage (GIDL) current, where the band bending at the drain side causes the flow of opposite carriers in the channel when the drain bias exceeds the gate bias. This significantly increases the off-state current. Fig. 9 depicts the transfer characteristics of the device as the drain bias varies. The results demonstrate that, unlike conventional Schottky barrier transistors, which are highly sensitive to drain bias, the off-state of the proposed Ge-RFET device is not affected by variations in drain bias. This can be attributed to the effect of the program gate on the appropriate band bending at the drain side, which mitigates the DIST effect. Furthermore, the appropriate band bending of the program gate in the off-state prevents the flow of opposite charge carriers in the channel, even with the low Schottky barrier height of Germanium. It is important to note that the increase in on-state current at elevated drain bias is primarily due to the enhancement of carrier velocity.

Figure 10 depicts the 2D variation contour of drain current as a function of the control gate and program gate voltage

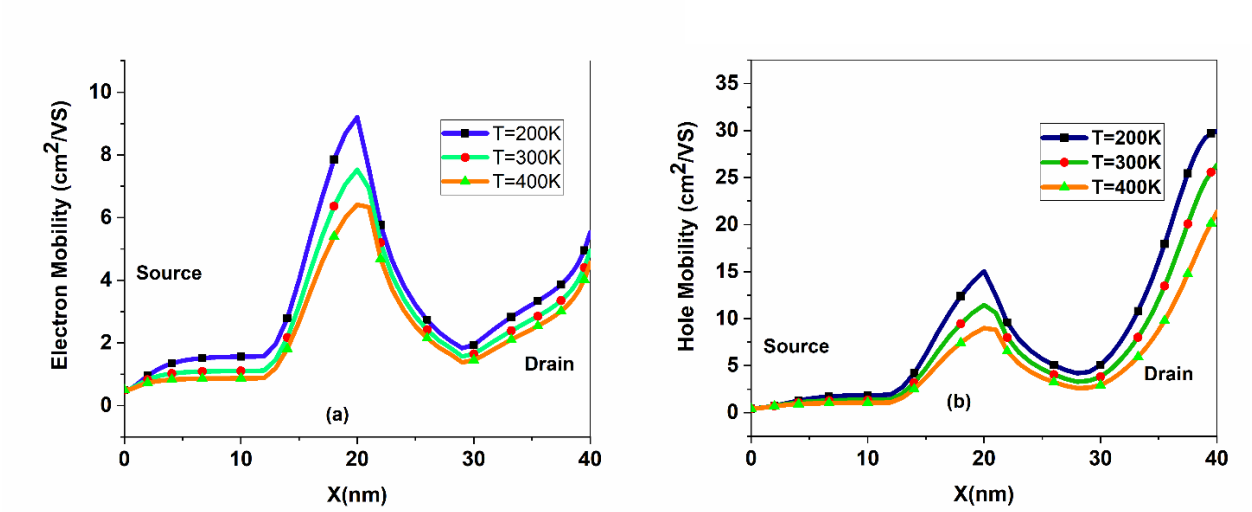

Fig. 8. Transfer characteristics of Ge-RFET as the temperatCarrier mobility along the device form source to drain as a function of temperature for (a) electron and (b) hole.

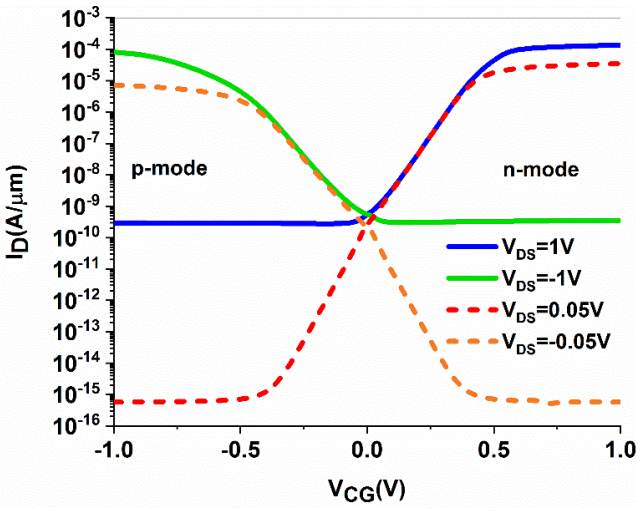

Fig. 9. Transfer charachteristics of Ge-RFET as the drain bias is varied for n-mode and p-mode operation.

values. The results indicate that the maximum on-state current is achieved in the top-right and bottom-left corners of the contour. This high drain current is attained when both the control gate and program gate have similar polarities and sufficient values. As mentioned earlier, the control gate modulates the carrier density in the channel and facilitates tunneling at the source-channel interface, while the program gate alters the band bending at the drain side to enable the transport of appropriate carriers (electrons or holes) in the channel. In the case of a positive control gate, electrons accumulate in the channel, and upon a positive value of the program gate, the appropriate band bending is created at the drain side to facilitate the transport of electrons along the channel. Similarly, for negative values of both the control gate and program gate, holes accumulate in the channel, and the band bending at the drain side directs the holes towards the drain electrode. However, the drain current decreases in the top-left and bottom-right corners of the variation matrix, where the control gate and program gate have dissimilar values. In this situation, carriers accumulate in the channel due to the applied control gate, but the opposite value of the program gate hinders the flow of carriers along the channel. The drain current is dependent on the values of the control gate and program gate, which enables the creation of a logic gate within a single device. The control gate and program gate act as inputs, with the drain current level serving as the output of the logic gate. A gate potential of 1.0 V signifies logic "1", while a gate potential of -1.0 V represents logic "0". A drain current lower than 10^{-12} A/μm indicates logic "0", whereas a drain current higher than 10^{-6} A/μm indicates logic "1". The simulations are carried out for V_{DS}=0.05 V. The 2D contour analysis demonstrates that the device can function as an XNOR gate.

The main feature of the proposed device, Ge-RFET, is that a two-input AND gate can be implemented on a single device. In the proposed AND gate, the control gate and drain electrode are considered as the input, and the drain current is considered as the output. The 2D variation contour of drain current as a function of the control gate bias and drain current bias is depicted in Fig.11. The program gate is considered constant at V_{PG}=1V. The findings indicate that when the drain current is zero and the control gate value is zero, there is no carrier flow through the channel, resulting in low drain

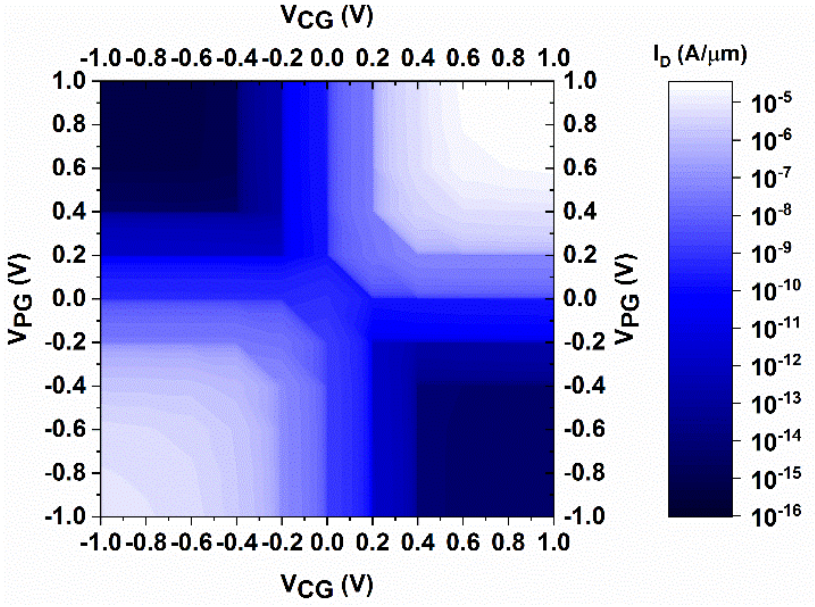

Fig. 10. contour of drain current variation as a function of control gate and program gate bias. The contour shows the XNOR logic gate operation.

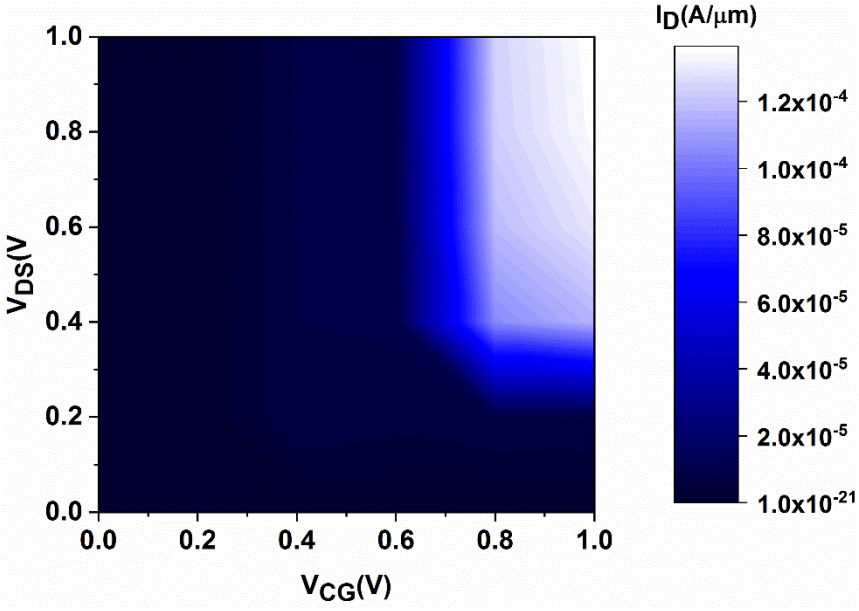

Fig. 11. 2D contour of drain current variation as a function of control gate and drain bias. The contour shows the AND logic gate operation.

Table 2. Truth table of the designed XNOR gate based on a single Ge-RFET.

Input 1: V_{CG}	Input 2: V_{PG}	Output: I_D (A)
0	0	1 ($I_D > 10^{-6}$)
0	1	0 ($I_D < 10^{-12}$)
1	0	0 ($I_D < 10^{-12}$)
1	1	1 ($I_D > 10^{-6}$)

current. Moreover, even with a high control gate value and zero drain bias, no current flow is anticipated. As the drain bias increases, with zero or low control gate bias, carriers do not accumulate in the channel to enhance the drain current. Only under high drain current and high control gate bias conditions does high drain current flow through the device from source to drain. In this particular design, the logic "0" is represented by a drain bias and control gate value of zero. Conversely, a high drain bias and control gate value are considered as the logic "1". Specifically, a drain current lower than 10^{-12} A/μm is classified as the logic "0", while a high drain current higher than 10^{-4} A/μm is classified as the logic "1". The 2D contour plot illustrates that the top right corner of the contour exhibits the highest drain current, which is achieved when both the control gate and drain current values are set to their highest values. Table 2 displays the truth table for the XNOR gate design, and Table 3 shows the truth table for the AND gate.

The electrical properties of the proposed Ge-RFET are evaluated in relation to other comparable structures within this domain to determine the device performance. The findings presented in Table 4 indicate that the on-state current of the device shows enhancement when compared to alternative structures. Nevertheless, the limited band gap of germanium necessitates additional efforts to enhance the on/off current ratio. Therefore, the integration of multi-gate devices along with ferroelectric gate oxide is suggested as a means to further optimize the functionality of the Ge-RFET.

4- Conclusion

This paper presents a comprehensive investigation into the electrical characteristics of a reconfigurable transistor that utilizes germanium as the channel material. The study reveals that the device exhibits similar behavior in both n-mode and p-mode operation. The gate work function is identified as a critical design parameter that effectively influences the symmetry of the n-mode and p-mode operation. The research findings indicate that a work function value of 4.35eV is the optimal choice for the proposed device. The device

Table 3. Truth table of the designed AND gate based on a single Ge-RFET.

Input 1: V_{CG}	Input 2: V_{PG}	Output: I_D (A)
0	0	0 ($I_D < 10^{-12}$)
0	1	0 ($I_D < 10^{-12}$)
1	0	0 ($I_D < 10^{-12}$)
1	1	1 ($I_D > 10^{-4}$)

Table 4. Electrical parameters of similar structures and the proposed Ge-RFET .

Reference	n-mode on-state current (p-mode)	on/off current ratio	Material	Bias value and configuration
[12]	0.553×10^{-6}A (1.39×10^{-6} A)	1.30×10^{7} (2.93×107)	Silicon (3D nanowire)	+1 V, -1V Schottky contact
[25]	1×10^{-6} A/μm (3×10^{-6} A/μm)	10^{2} (10^{3})	Silicon (3D nanowire)	+3 V, -3V Schottky contact
[9]	178×10^{-6} A/μm (114×10^{-6} A/μm)	17.8×10^{5} (11.4×10^{5})	Silicon (3D nanowire)	+1.5 V, -1.5V Schottky contact
[16]	1×10^{-5} A (1×10^{-6} A)	1×10^{9} (1×10^{8})	Silicon (3D nanowire) Ferroelectric gate oxide	+0.8 V, -0.8V Schottky contact
This work	1.3×10^{-4} A/μm (8.5×10^{-5} A/μm)	1.34×10^{5} (2.35×10^{5})	Germanium (2D double gate)	+1 V, -1V Schottky contact

performance deteriorates at high temperatures due to its low band gap and low Schottky barrier height. Furthermore, the study demonstrates the implementation of a two-input XNOR and two-input AND gate on a single Ge-RFET device. This approach offers numerous advantages, including area efficiency, reduced power consumption, flexibility, and reconfigurability. These benefits greatly contribute to the advancement of modern digital circuit design.

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