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Two-step Dynamic Foreground Auto-Calibration of Binary Weighted Current Steering DAC

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ABSTRACT: This paper presents a novel and versatile calibration technique designed for application in Binary Weighted Current Steering Digital-to-Analog Converters (DACs). The primary motivation for this work stems from the limited availability of calibration methods that address matching accuracy, despite the widespread adoption of such converters. The proposed technique facilitates automatic calibration of the DAC as required, leveraging two distinct clock signals: a low-frequency clock for calibration and a high-frequency clock for standard operational modes. The calibration process employs a unique and algorithmically-driven calibration block to systematically eliminate transistor mismatch-induced current errors across all current sources. A configurable triple-path scheme is implemented to steer previously calibrated least significant bit (LSB) currents into the summing node, which subsequently updates the reference current. This updated reference is then used to calibrate the next most significant bit (MSB) current. To validate the effectiveness of the proposed technique, simulations were conducted for a 10-bit DAC using Cadence tools with TSMC 180nm CMOS technology. The DAC was subjected to an intentionally introduced current error of up to 125 LSB in the binary-weighted current blocks. The simulation, performed at a sampling frequency of 125 MHz with a 1.8 V supply voltage and a 500 nA LSB current, demonstrated the robustness and accuracy of the proposed calibration method.

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1- Introduction

High speed, linearity, and power efficiency are among the primary advantages of current-steering digital-to-analog converters (DACs). These converters are widely used in applications such as WLAN, UMTS, and GSM [1]. Binary-weighted current-steering DACs are particularly favored for medium-performance systems [2-4] Due to their compact architecture, low power consumption, and elimination of additional circuitry required in segmented architectures, such as binary-to-thermometer converters and large decoders [5].

However, the performance of DACs, both static and dynamic, is highly sensitive to transistor matching accuracy [6], an issue that is particularly critical for binary-weighted DACs [7, 8]. Various techniques have been proposed to address matching challenges in segmented architectures, including dynamic element matching (DEM) [9], randomization methods [10], DMOS-enabled designs [11],, layout optimization [12, 13],, self-calibration [14], and random switching sequences [10]. Additionally, methods such as deglitching schemes [10, 15], swing-reduced drivers (SRD) [16], and variable voltage levels [17] have been employed to enhance transient performance.

Despite the benefits of binary-weighted current-steering DACs, the lack of effective calibration mechanisms limits their broader adoption. Existing calibration techniques [18, 19] often rely on parallel structures with independent reference blocks for adjustment. While these methods are fast, they inherit the same random error characteristics as the binary current source blocks. In [20] An initial dynamic foreground calibration idea was introduced, offering acceptable performance, and this work builds on that foundation.

This paper proposes a novel foreground serial calibration technique for dynamically calibrating binary-weighted current-steering DACs. The architecture includes 5-bit coarse and 5-bit fine calibration for LSB and MSB blocks, respectively. By employing a voltage comparator to detect the cross point of the calibration block's output voltage with a constant reference, the method effectively eliminates error sources and enhances DAC performance.

The paper is organized as follows: Section 2 explains the proposed structure's operational principles, covering (A) Conceptual Analysis, (B) Circuit-Level Analysis, (C) Coarse Calibration Control Signal Generator, and (D) Fine Calibration Control Signal Generator. Section 3 presents simulation results, and Section 4 concludes the paper.

2- Principle of Operation

The performance of digital-to-analog converters (DACs) is significantly affected by statistical variations in process, voltage, and temperature (PVT). These variations degrade

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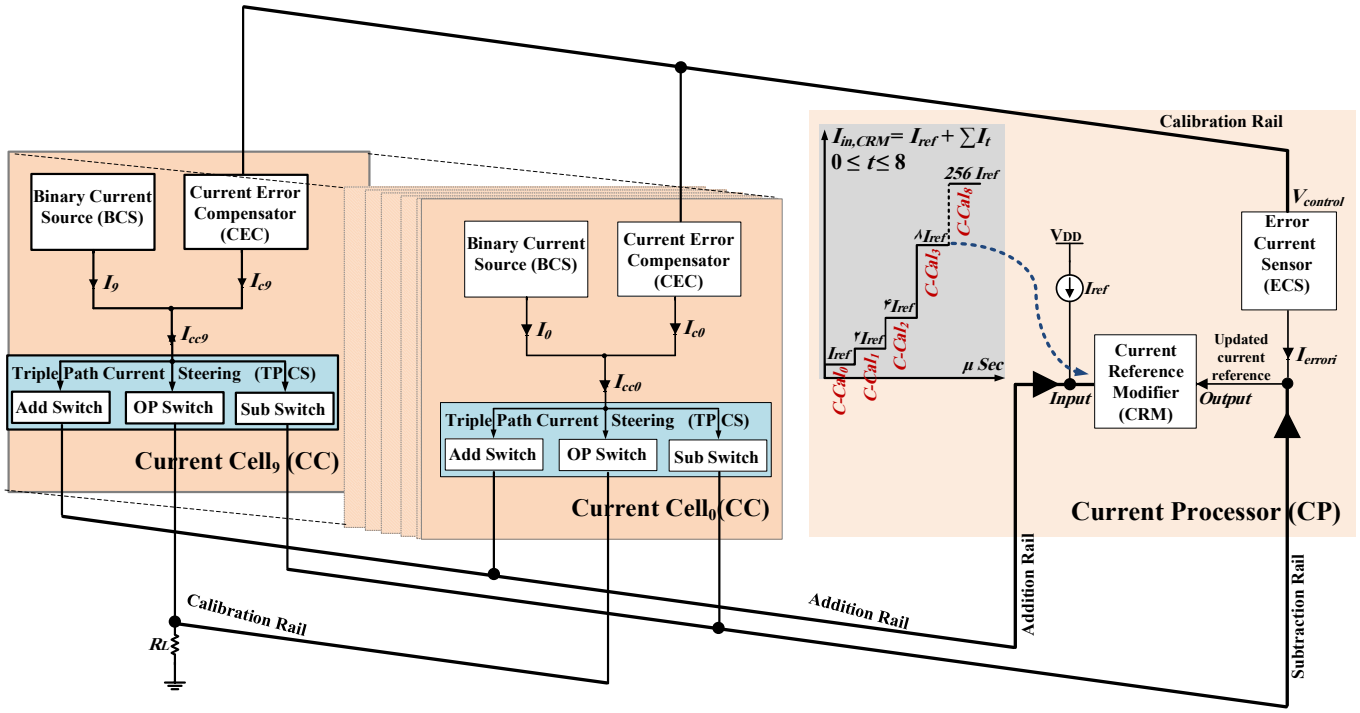

Fig. 1. The simplified block diagram of the proposed serial calibration scheme.

the precision of signal conversion and reduce the overall system accuracy by impairing signal transfer and processing capabilities. To mitigate these issues, a two-phase operational approach is proposed. The first phase involves preprocessing calibration to address random PVT-induced errors, followed by a normal operation phase for data conversion. The proposed calibration scheme operates intermittently and can be initiated as needed.

2- 1- Conceptual analysis of the Calibration Scheme

Overview:

Fig. 1 presents the simplified block diagram of the proposed serial calibration scheme. This approach employs a unique current reference block, I_{ref}, which is utilized at regular intervals to sequentially calibrate binary-weighted current source blocks (I_i) in ascending order from the least significant bit (LSB) to the most significant bit (MSB). The reference current I_{ref} is equivalent to the calibrated LSB current.

While conventional parallel calibration schemes may appear faster, the proposed serial calibration method is advantageous as calibration occurs infrequently and can be executed during idle periods where active input data are not available. This approach not only avoids significant limitations but also achieves higher precision, which is a considerable benefit.

Block Diagram and Functional Details:

The calibration system comprises ten uncalibrated binary current sources (BCS) and ten current error compensators (CEC) linked to a current processor (CP) via a triple-path current steering (TPCS) block. Each TPCS block incorporates three MOS switches—*Add*, *Sub*, and *Op*—to manage current flow. The CP functions as a high-performance current mirror, where the input signal is the sum of I_{ref} and all previously calibrated LSB currents. This summed signal is fed through an "addition rail" controlled by *Addt* switches ($0 \le t \le 80$).

The mirrored current, referred to as the "updated reference current," is subtracted from the next uncalibrated BCS (BCS_{t+1}) current, I_t, via a "subtraction rail" connected by Sub_{t+1} switches. The resulting error current is transmitted to the error current sensor (ECS), which generates a control voltage ($V_{control}$) to regulate the compensation current (I_{ct}) injected by the CEC.

Calibration Process

The calibration process is illustrated in Fig. 1, which can be comprehended as follows.

Initially, I_{ref} is used to calibrate the uncalibrated LSB current source (I_0). During the first calibration phase, a compensation current I_{c0} is added to I_0, ensuring the total current equals I_{ref}. In subsequent phases, the calibrated currents I_0+I_{c0} and I_{ref} are used to calibrate I_1, resulting in $2I_{ref}$. This process continues hierarchically, calibrating each block from LSB to MSB until all components are calibrated.

Once calibration is complete, the system transitions to normal operation. During this phase, calibration paths are disconnected from subtraction and addition rails, and the calibrated currents are routed to appropriate loads through the "load rail," determined by the input data. Special

considerations, such as voltage stress management of the Current Reference Modifier (CRM) block during calibration, are addressed using the Initial Value Adjuster (IVA).

2- 1- 1- Detailed Architecture

The complete architecture of the calibration scheme is illustrated in Fig. 2. The system comprises the following major components:

1- Current Processor (CP) Block
- Current Reference Modifier (CRM)
- Error Current Sensor (ECS)
- Initial Value Adjuster (IVA)

2- Current Cell (CC) Block
- Coarse Current Error Compensator (CCEC)
- Fine Current Error Compensator (FCEC)
- Binary Current Source (BCS)
- Triple Path Current Steering (TPCS)
- Differential Structure (DS) with Built-in Intrinsic Deglitcher (BID)
- Current Buffer (CB)
- Coarse Calibration Control Signal Generator (CCCSG)

3- Coarse Calibration Digital Core (CCDC)
- Frequency Adjustment (FA)
- Coarse Sequence Counter (CSC)
- Micro Time Interval Generator (MTIG)
- Addition Control (AC)
- Subtraction Control (SC)
- Normal Operation Control (NOC)
- Fine Calibration Control Signal Generator (FCCSG)

4- Fine Calibration Digital Core (FCDC)
Fine Sequence Counter (FSC)
- Fine Calibration Thermometer Coder (FCTC)
- Fine Calibration Mask (FCM)
- Nano Time Interval Generator (NTIG)

5- Voltage Comparator (VC)
6- Latch Block
- Clock/Data Mask (C/D Mask)

2- 1- 2- Operation and Timing

The proposed 10-bit DAC structure ($0 \le t \le 9$) consists of coarse calibration for 5-LSB ($0 \le i \le 4$) and fine calibration for 5-MSB ($5 \le k \le 9$) blocks. Among the aforementioned sub-blocks, CCEC and CCCSG are used for coarse calibration, VC, FCEC, and FCCSG are used for fine calibration, while all the other sub-blocks are used for both calibrations. In general, the $V_{control}$ voltage mentioned above is exploited to charge the capacitors, C_i and C_k to the desired voltage for which the I_{Ci} and I_{Ck} currents are injected by the voltage-controlled current sources (VCCS), and calibrate the BCS sub-blocks. This is accomplished by controlling the $Switch_i$ and $Switch_k$ switches, with the appropriate $C\text{-}Cal_k$ clock-based digital pulses that are generated by the CCCSG block,

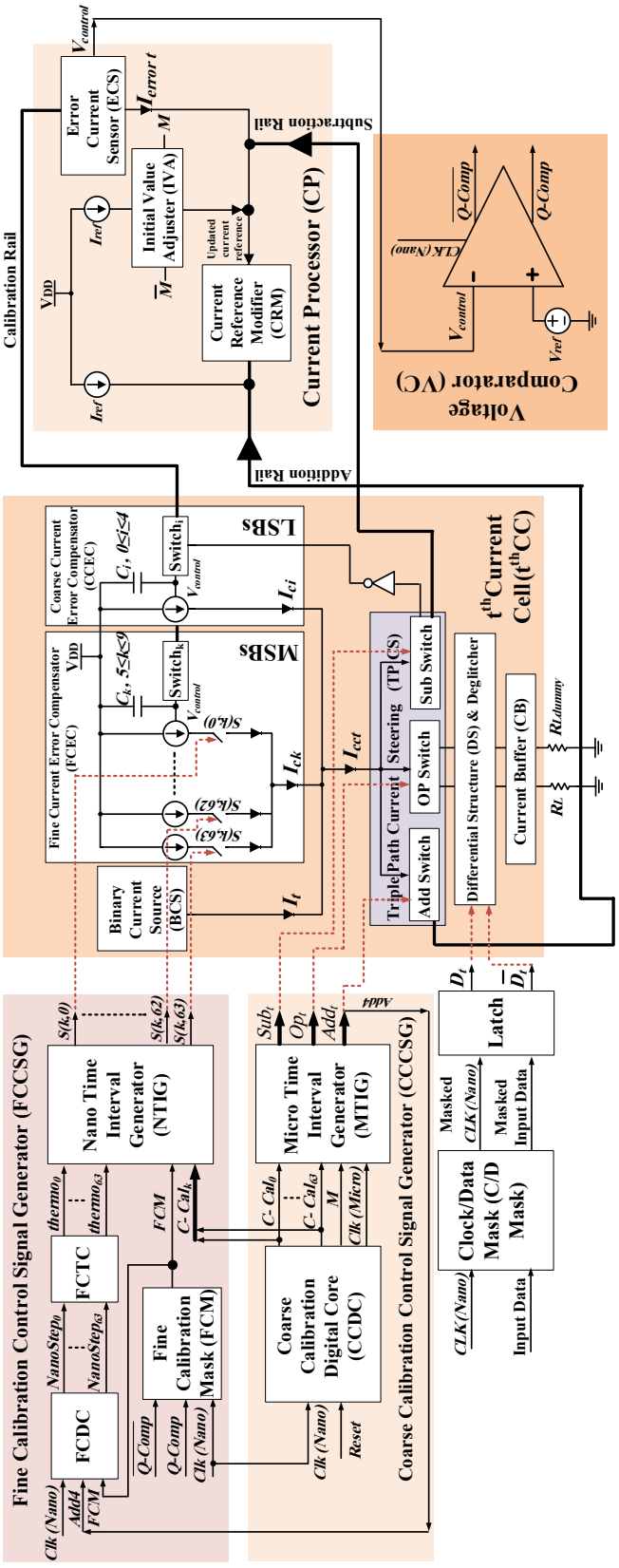

Fig. 2. Proposed calibration architecture block diagram (in detail).

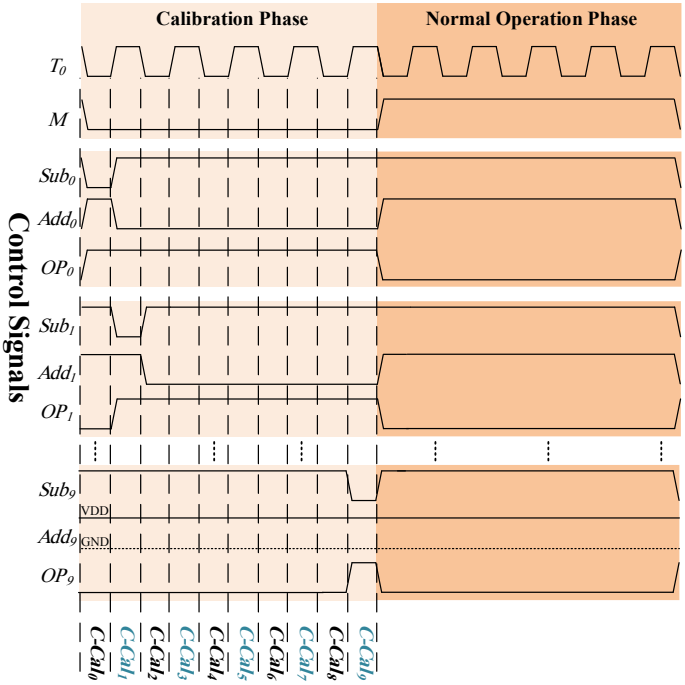

Fig. 3. The signals used to handle the triple path current steering sub-block.

and controlling the fine VCCS switches with the *S(k,j)* digital pulses that are generated by the FCCSG block, where $0 \le j \le 63$. Since the capacitors require a sufficiently large time to store the $V_{control}$, thus suitable time intervals must be produced by the MTIG sub-block for so-called coarse calibration. The coarse calibration time interval is selected to be about 1 µs in this research. Since 64 VCCS is utilized for fine calibration, which must be handled during the abovementioned 1 µs, thus each fine current source must be treated within the 16ns (1 µs=64×16ns). For fine calibration of the 5-MSB bits, a determined number out of 64 VCCS currents is selected by the Voltage Comparator (VC) block to produce an acceptable I_{Ck}.

The VC block compares $V_{control}$ which is modified by I_{Ck} with V_{ref} every 16ns and decides to select another VCCS current or not.

2- 1- 3- Signal Analysis

Fig. 3 outlines the signals used in the TPCS sub-block:

- **Mode Signal (*M*):** Specifies calibration (*M*=0) or normal operation (*M*=1).
- **Subtraction Signals (Sub_t):** Control subtraction of BCS_t current to the subtraction rail.
- **Addition Signals (Add_t):** Direct BCS_t current to the addition rail.
- **Operation Signals (OP_t):** Route BCS_t current to the load rail during normal operation.

Identical calibration intervals ($C{-}Cal_t$, "Coarse Calibration of t^{th} stage") are assigned for each BCS_t block ($0 \le t \le 9$), completing the coarse calibration process.

2- 2- Circuit level analysis

The transistor-level implementations of the 5-LSB coarse calibration and 5-MSB fine calibration architectures are depicted in Figs. 4 and 5, respectively. This section examines the design requirements and performance of these structures in detail. The BCS_t sub-blocks are regulated cascode-enhanced current mirrors, designed to supply the required currents of $I_t = 2^t \times I_{LSB}$ to the load. Any deviation of this current from the ideal value due to the PVT variations can adversely affect the overall static and dynamic performance of the DAC.

To address this issue, a compensation current equal to I_{ct} is generated during the coarse/fine calibration phases and injected into the summing node.

2- 2- 1- Coarse Calibration Phase

The coarse calibration targets the 5-LSB ($0 \le i \le 4$) blocks, as illustrated in Fig. 4. During the time interval $C\text{-}Cal_0$, the control signals configure the circuit such that Sub_0 is low, Add_0 is high, and OP_0 is high. Consequently, PMOS transistor M_{sub0} is turned ON, while M_{add0} and M_{op0} remain OFF. This configuration injects the sum of I_{c0} (initially zero) and I_0 into the subtraction rail: $I_{sub\_rail}=I_0+I_{c0}$. The subtraction rail interfaces with the output of the Current Reference Modifier (CRM), a regulated cascode current mirror that sums currents from the addition rail I_{add_rail} and the reference current I_{ref}. The CRM then outputs the updated reference current: $I_{ref\_updated} = I_{add\_rail}+I_{ref}$. At $C\text{-}Cal_0$, since all M_{addi} transistors are OFF, I_{add_rail} is zero. The difference between $I_{ref\_updated}$ and I_{sub_rail}, defined as $I_{error}=I_{ref}-I_0-I_{c0}$, is delivered to the Error Current Sensing (ECS) sub-block.

The ECS employs two diode-connected PMOS

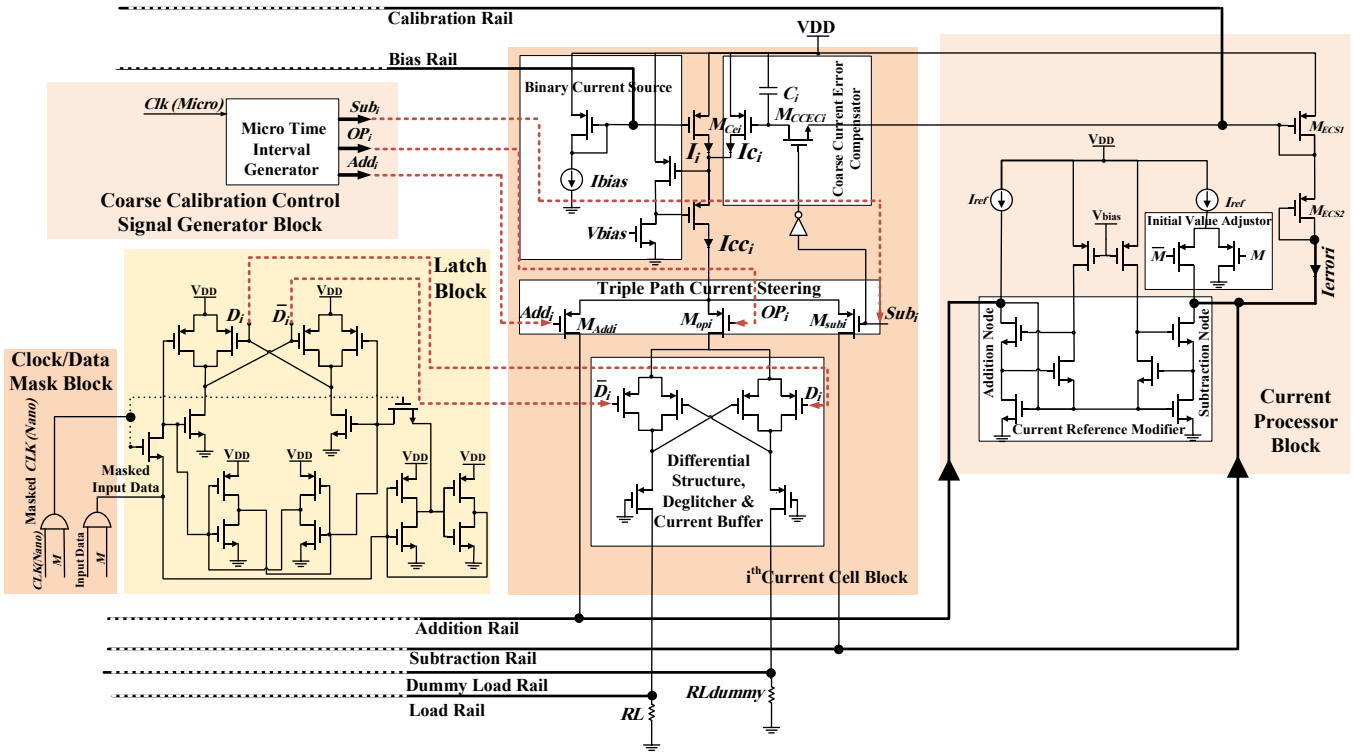

Fig. 4. The transistor level implementation of the 5-LSB bit coarse calibration architectures.

transistors, M_{ECS1} and M_{ECS2}. M_{ECS1} generates the control voltage $V_{control}=|V_{gs,ECS1}|$, which is stored in capacitor C_0. Meanwhile, M_{ECS2} adjusts the DC voltage at the CRM output. During *C-Cal*$_0$, the NMOS transistor M_{CCEC0}, controlled by calibration signals, connects $V_{control}$ to C_0. As V_{C0} increases, the compensation current I_{c0}, delivered by M_{Ce0}, grows. This reduces I_{error} and the increment rate of V_{C0}, resulting in an exponential decay of the error. To minimize calibration time ($\tau_i=R_{ONi}\times C_i$), the dimensions of M_{CCECi} are optimized. Each calibration interval (*C-Cal*$_i$) is approximately 1µs to allow complete capacitor charging. The process continues until I_{error} stabilizes at a negligible value in comparison with I_{ref}, ensuring $I_{ref} \simeq I_{cc0}=I_0+I_{c0}$, completing the calibration of the first Current Cell (CC) block.

For *C-Cal*$_1$, Sub_1 is low, Add_1 is high, and OP_1 is high, enabling M_{sub1} while turning OFF M_{add1} and M_{op1}. In this phase, Sub_0 is deactivated, disconnecting I_{cc0} from the subtraction rail. The rail now carries $I_{sub\_rail}=I_1+I_{c1}$ for calibration. Simultaneously, Add_0=0 activates M_{add0}, directing I_{cc0} to the addition rail ($I_{add\_rail}=I_{cc0}=I_{ref}$). The CRM then updates the reference current: $I_{ref\_updated} = I_{add\_rail}+I_{ref} = I_{cc0}+I_{ref} = 2I_{ref}$. The ECS sub-block determines $I_{error}=I_{ref\_updated}-I_{sub\_rail}$, and the calibration of C_1 proceeds in the same manner, achieving $I_{cc1}=I_1+I_{c1}\simeq 2I_{ref}$.

The process is repeated for the remaining LSB blocks. For *C-Cal*$_4$, all Sub_i signals except Sub_4 are high, yielding $I_{sub\_rail}=I_{cc4}$. Similarly, all Add_i signals except Add_4 are low, producing $I_{add\_rail}= I_{cc3}+\ldots+I_{cc1}+I_{cc0}=(2^4-1)\times I_{ref}$. The CRM updates the reference current to $I_{ref\_updated} = I_{add\_rail}+I_{ref}=2^4\times I_{ref}$. The error current $I_{error}=I_{ref\_updated}-I_{sub\_rail}= 2^4\times I_{ref}-I_{cc4}$ ensures precise calibration.

2- 2- 2- Fine Calibration Phase

Fine Calibration is applied to the 5-MSB ($5\le k\le 9$) blocks (Fig. 5). Although the fine calibration utilizes the same infrastructure that was previously realized for coarse calibration, there is a main difference between these calibrations in terms of generating the error compensation currents. In other words, comparing the transistor level implementations of the coarse and fine calibration schemes that are shown at Figs. 4 and 5, respectively, it is revealed that, instead of using only one coarse compensation current (pure coarse calibration) which is generated by M_{Cei} ($0\le i\le 4$ for 5-LSB block) transistor during the *Micro step k* coarse calibration time interval, "*j*" small size transistors, $M_{Fe}(k,j)$, are considered, each producing a selectable fine compensation current, *I(k,j)*, during *Nano step* (*k*,*j*) fine calibration time intervals (embedded fine calibration). As mentioned before, All *Micro step*s, i.e., *C-Cal*$_t$ $0\le t\le 9$, are equal with about 1µSec. Since the sampling period is 8 nSec, devoting two clock periods, i.e. *Nano step*=16nSec, for the fine calibration, "*j*" is obtained 64 (64 × 16 nSec = 1.024 µSec ≃ 1 µSec).

The time scheduling scheme is depicted in Fig. 6 in which, for 5-MSB bits, the coarse *Micro step k* time intervals are split into 64 fine *Nano step* (*k*,*j*) time intervals.

After the pure coarse calibration for 5-LSB blocks, the

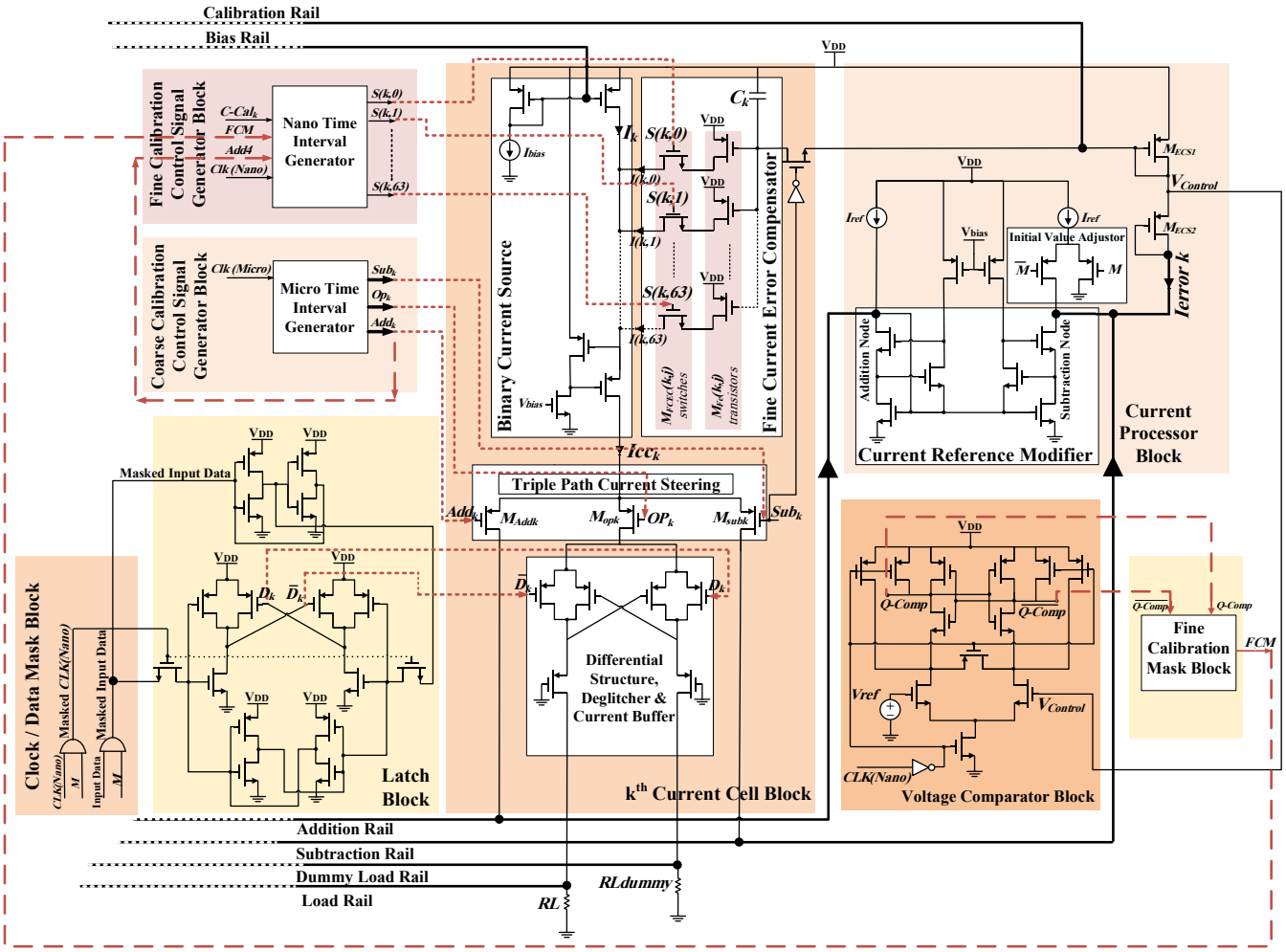

Fig. 5. The transistor level implementation of the 5-MSB bit fine calibration architectures.

micro-step k control signals, namely, Add_k, Sub_k and OP_k preserve their previous trend for fine calibration of 5-MSB blocks. Therefore, the TPCS sub-block is already configured, and the fine calibration scheme can be started. All 64 $M_{Fe}(k,j)$ transistors ($0 \le j \le 63$) are connected to the circuit through $M_{FCEC}(k,j)$ switches.

All switches are initially off and based on the flowchart given at Fig. 7 are turned on one after another during the *Nano step* (k,j) time intervals to contribute to the overall compensation current.

The flowchart of the fine calibration procedure describes how a determined number out of 64 $M_{FCEC}(k,j)$ switches are turned on for k^{th} block. As the flowchart shows, the fine calibration starts from 5th bit (k=5) and continues to the 9th bit (k=9). For each k, to partially compensate the BCS_k current error due to the process mismatches, the fine unary current of $I(k,j)$ is injected to it during the *Nano step (k,j)* time interval.

During each *Nano step (k,j)*, the control voltage, $V_{control}$, of the ECS sub-block is compared with the reference voltage, V_{ref}, by the voltage comparator (VC) block, to decide whether the calibration is well done and the fine calibration can be terminated, or the calibration must continue to inject some more current into the circuit.

If the calibration condition is not achieved, the same will continue up to j=63 to try to fully calibrate the mentioned block. Note that the amount of error that can be compensated is limited to $64 \times I(k,j)$.

2- 2- 3- Normal Operation Phase

After completing the calibration process, the value of M becomes high, initiating the normal operation phase. In this phase, all M_{subt} and M_{addt} transistors are turned OFF, while M_{OPt} transistors simultaneously turn ON. Consequently, no current flows through I_{sub_rail} and I_{add_rail}. However, without appropriate measures, the error current (I_{error}) would equal the reference current (I_{ref}), which is significantly large. This could cause the transistors at the CRM's output to enter the triode region due to the high $V_{gs,ECS1+}V_{gs,ECS2}$. Such a condition would increase the calibration latency whenever recalibration is needed.

To mitigate this issue, the IVA sub-block, controlled by M and activated during the normal operation phase (M=1), ensures that I_{ref} is routed to the CRM's output node. This keeps I_{error} minimal, maintaining the CRM in standby mode

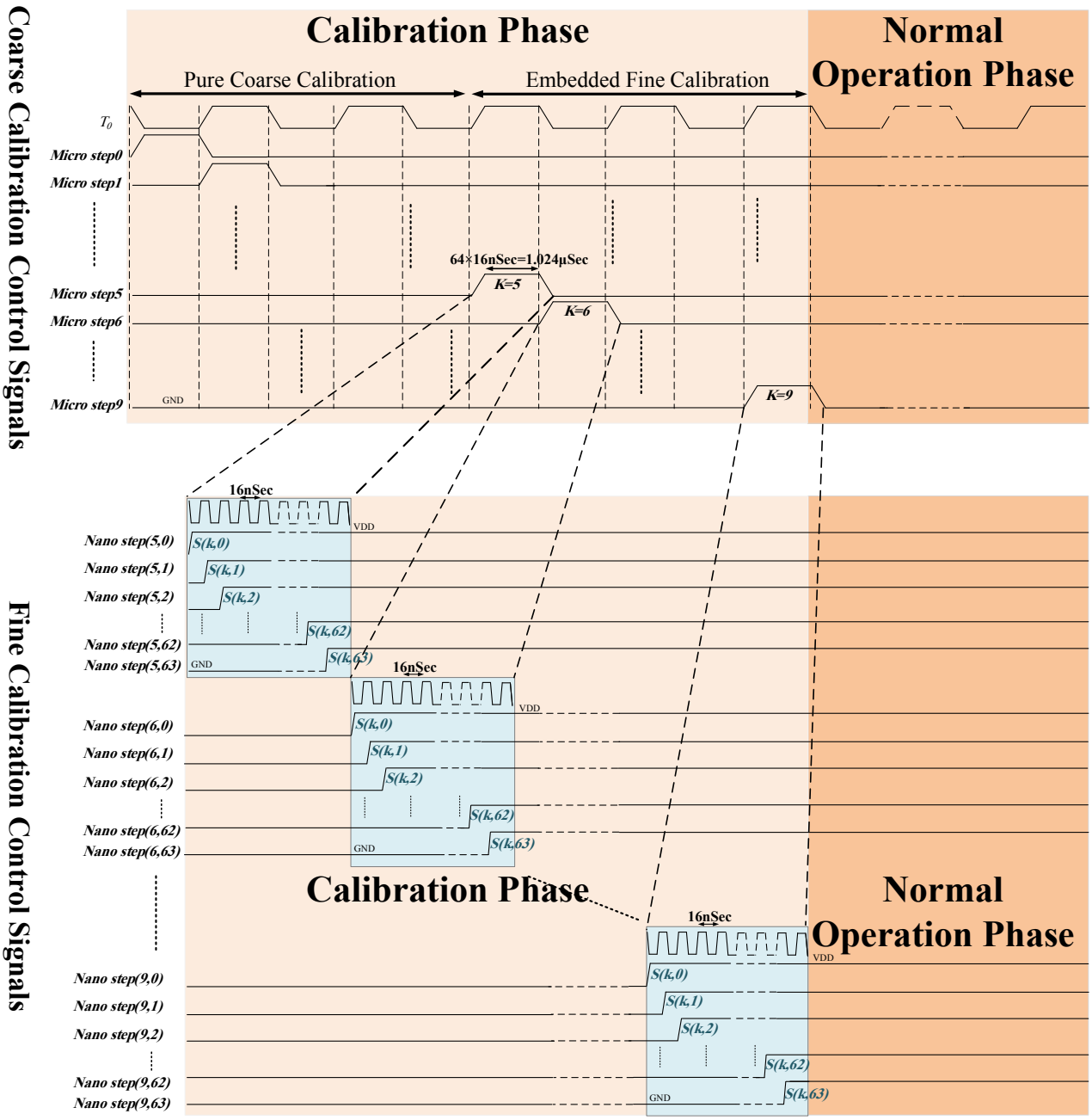

Fig. 6. Splitting the coarse Micro step k time interval into the fine Nano step (k,j) time intervals for 5-MSB bits.

and ready for recalibration. Since the M_{QPt} transistors are all ON, the current from each CC block flows through the Differential Structure (DS) sub-block. These currents are directed to the corresponding load rail based on the input data signals from the latch sub-block [21]. A conventional single-transistor Current Buffer (CB) sub-block is also included to handle glitches effectively. During normal operation, the data signals (D_t) direct the calibrated currents to the appropriate load resistances. Fig. 8 illustrates the overall 10-bit proposed binary-weighted current-steering DAC, which integrates the coarse and fine calibration architectures shown in Figs. 4 and 5.

The following subsections illustrate the digital blocks that generate appropriate *Micro step k* and *Nano step* (*k,j*) signals, with Coarse (Fig. 9) and Fine (Fig. 10) Calibration Control Signal Generator, respectively. These signals are used to configure and control the overall calibration schemes of the proposed DAC.

2- 3- Coarse Calibration Control Signal Generator

The primary innovation of the proposed architecture, which ensures error-free calibration of the Binary Weighted Current Steering (BWCS) DAC, lies in utilizing a single CP block to calibrate all its BCS blocks.

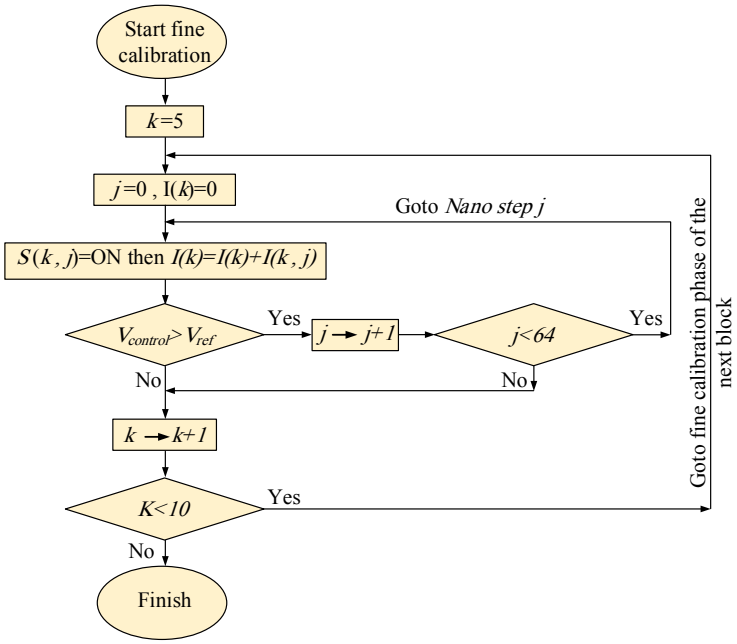

Fig. 7. The flowchart of the fine calibration procedure

This necessitates precise control and direction of current signals through the appropriate Triple Path Current Steering (TPCS) sub-block, as described earlier. To achieve this, a Coarse Calibration Control Signal Generator (CCCSG) block is implemented, comprising a Micro Time Interval Generator (MTIG) and a Coarse Calibration Digital Core (CCDC), as depicted in Fig. 9. These sub-blocks generate signals based on the time sequence shown in Fig. 11a, producing the Micro step *t*-time interval-based signals: *C-Cal*$_t$ (Fig. 11b), Addition (Fig. 11c), Subtraction (Fig. 11d), and Normal Operation (Fig. 11f).

The MTIG generates Addition Control (AC), Subtraction Control (SC), and Normal Operation Control (NOC) signals to manage the current paths, as explained later. The CCDC consists of two sub-blocks: the Frequency Adjustment (FA) sub-block and the Coarse Sequence Counter (CSC) sub-block. The FA sub-block includes seven T Flip-Flops (TFFs) arranged in series to form a frequency divider. Meanwhile, the CSC sub-block comprises a 4-bit Up-Counter and a 4×16 Decoder. Each calibration step requires sufficient time while accommodating input data frequencies as high as the Nyquist frequency. Therefore, the proposed architecture employs two clock frequencies: a nano clock (CLK_n) for fine calibration and normal operation (8nSec and 16nSec, respectively, as discussed in the next subsection), and a micro clock (CLK_μ) of 1.024μSec for coarse calibration.

The DAC's primary sampling clock, CLK_n (125 MHz), is fed into the FA sub-block to generate its divided version, CLK_μ (~1 MHz), for use within the CCDC. The CSC sub-block produces uniform micro-step *k*-time intervals, *C-Cal*$_t$, for calibrating each BCS block during the calibration phase. The counter's clock pulse is derived from a 2×1 multiplexer. The multiplexer's input selection is controlled by a *Reset* signal, which is typically at GND and transitions to V_{DD} for brief periods when calibration is initiated. The multiplexer inputs are as follows:

$$\text{Reset} = \begin{cases} 0, & I_0 = \overline{M}\ .CLK_\mu \\ 1, & I_1 = CLK_\mu \end{cases} \quad (1)$$

The signal *M* (*M*=T_1 and T_3) is used to indicate the end of the calibration phase. For the 10-bit DAC, the Up-Counter increments from zero to ten using a masked clock pulse (I_0), with the corresponding decoder output becoming high at each step.

When the counter reaches ten, represented as (T_3 T_2 T_1 T_0)$_2$=(1010)$_2$, the Normal Operation phase control signal is activated. At this point, *M* transitions from GND to V_{DD}, initiating the normal operation phase (Fig. 11a). This transition ensures the counter remains at (1010)$_2$ by setting I_0=GND, preserving the normal operation condition.

For DAC recalibration, the Reset signal is switched to V_{DD}, allowing the unmasked clock pulse (I_1) to be applied to the counter clock input. Simultaneously, the counter is reset to zero, enabling the calibration process to restart.

2- 3- 1- Signal Analysis for Path Control

During normal operation, the Up-Counter holds a value of (1010)$_2$. When Reset=V_{DD} is applied, the counter resets to zero, causing the decoder's O_0 output to go high while all other outputs remain low. The subtraction, addition, and operation control signals for this calibration time interval are as follows:

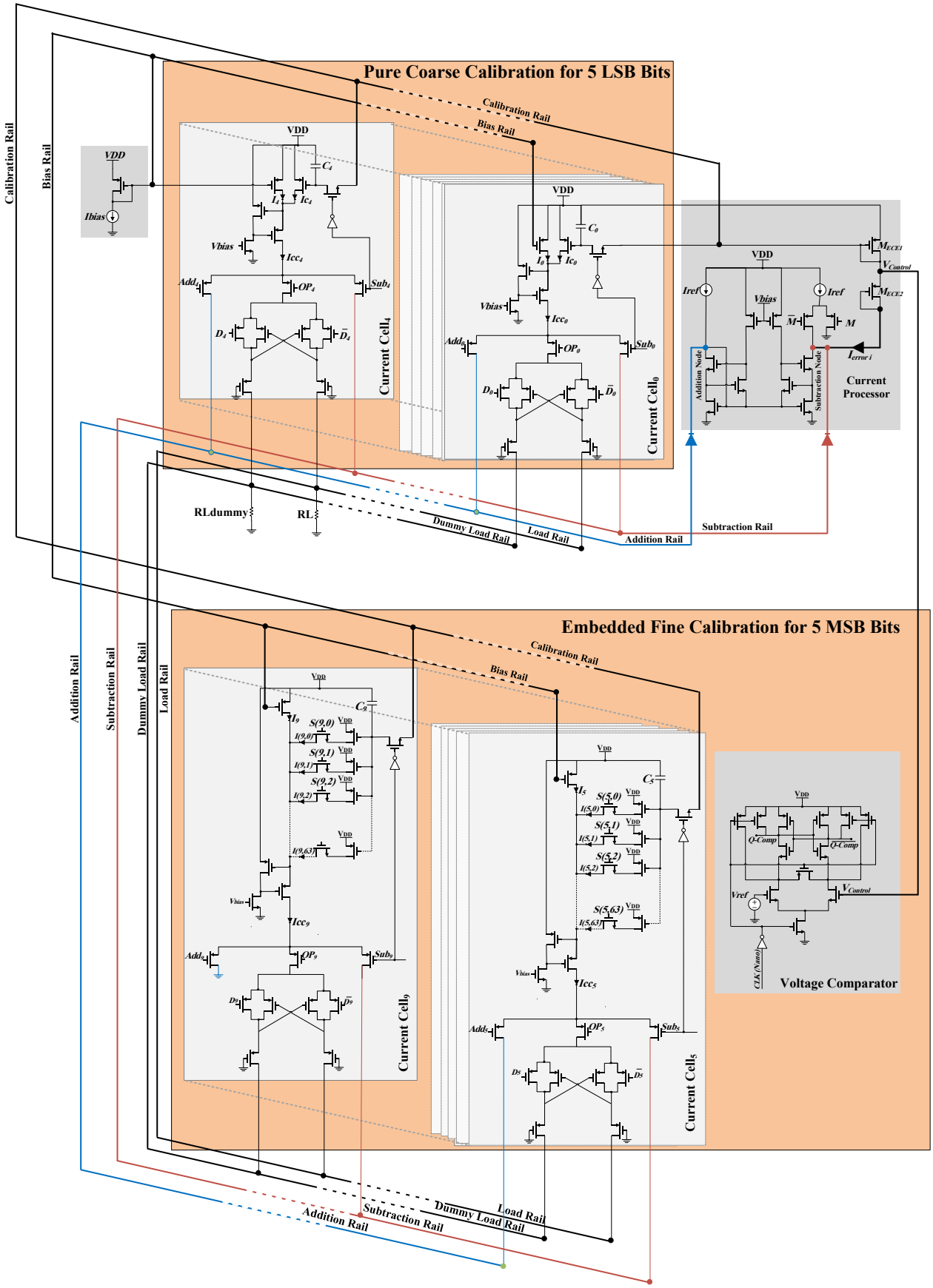

Fig. 8. Overall 10-bit proposed binary weighted current steering DAC.

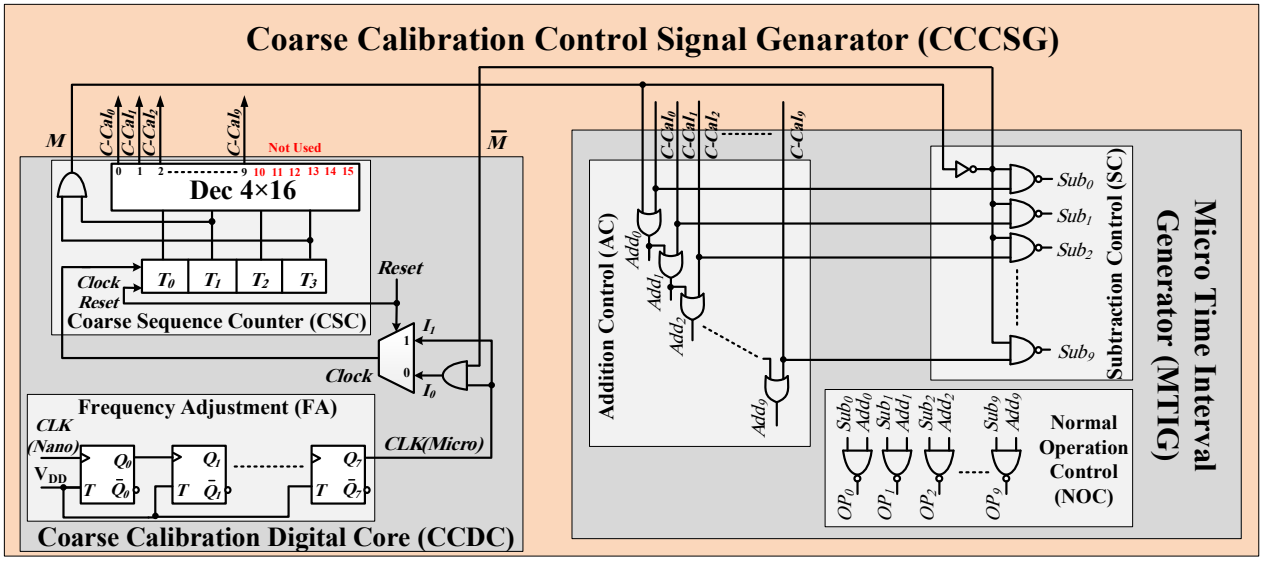

Fig. 9. Micro step k coarse calibration control signal generator.

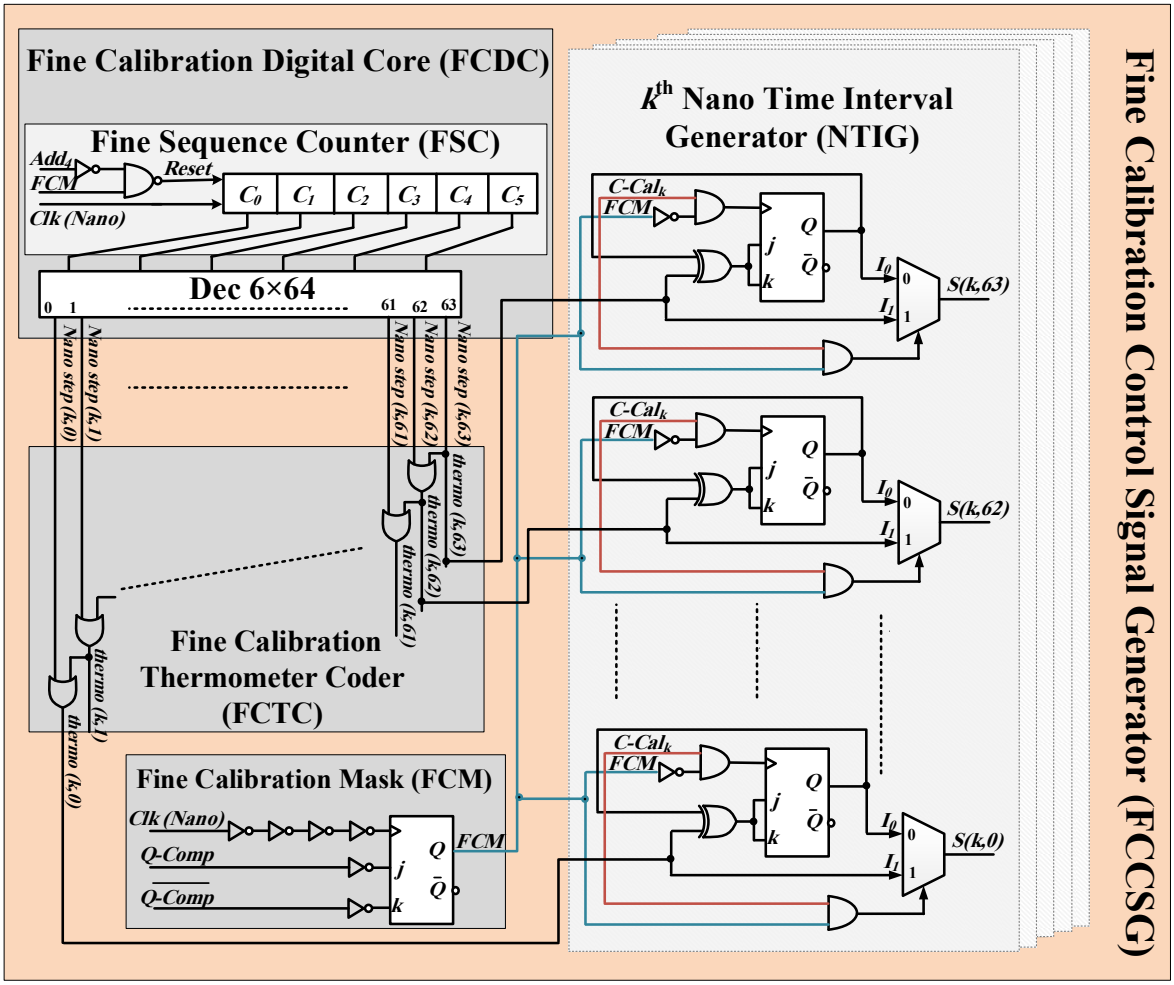

Fig. 10. Nano step (k,j) fine calibration control signal generator.

Time Interval *C-Cal*$_0$:

$$\begin{aligned} &Sub_0 = \overline{\overline{M}.O_0} = \text{GND} && \text{(Refer to } C\text{-}Cal_0 \text{ at Fig.11d)} \\ &Add_0 = M + O_0 = \text{V}_{\text{DD}} && \text{(Refer to } C\text{-}Cal_0 \text{ at Fig.11e)} \\ &Op_0 = \overline{sub_0.add_0} = \text{V}_{\text{DD}} && \text{(Refer to } C\text{-}Cal_0 \text{ at Fig.11f)} \end{aligned} \quad (2)$$

Time Interval *C-Cal*$_1$:

$$\begin{aligned} &Sub_0 = \text{V}_{\text{DD}} && \text{(Refer to } C\text{-}Cal_1 \text{ at Fig.11d)} \\ &Add_0 = \text{GND} && \text{(Refer to } C\text{-}Cal_1 \text{ at Fig.11e)} \\ &Op_0 = \text{V}_{\text{DD}} && \text{(Refer to } C\text{-}Cal_1 \text{ at Fig.11f)} \\ &Sub_1 = \overline{\overline{M}.O_1} = \text{GND} && \text{(Refer to } C\text{-}Cal_1 \text{ at Fig.11d)} \\ &Add_1 = M + O_1 + O_0 = \text{V}_{\text{DD}} && \text{(Refer to } C\text{-}Cal_1 \text{ at Fig.11e)} \\ &Op_1 = \overline{sub_1.add_1} = \text{V}_{\text{DD}} && \text{(Refer to } C\text{-}Cal_1 \text{ at Fig.11f)} \end{aligned} \quad (3)$$

According to Eq. (2), Add_0 and Op_0 are V_{DD}, deactivating the PMOS transistors they control, while Sub_0 is GND, enabling M_{sub0}. As a result, BCS_0 is configured for calibration as described earlier.

Eq. (3) shows that Sub_0, Op_0, Add_1, and Op_1 are V_{DD}, turning off the associated PMOS transistors. Meanwhile, Sub_1 is GND, enabling M_{sub1}, and BCS_1 is configured for calibration. Here, Add_0 is GND, connecting M_{add0} to the Addition Rail to sum with I_{ref}, generating the updated reference current $2\times I_{ref}$.

Time Interval *C-Cal*$_t$:

$$\begin{aligned} &Sub_z = \text{V}_{\text{DD}}, \quad z = 0,...,t\text{-}1 && \text{(Refer to } C\text{-}Cal_t \text{ at Fig.11d)} \\ &Add_z = \text{GND}, \quad z = 0,...,t\text{-}1 && \text{(Refer to } C\text{-}Cal_t \text{ at Fig.11}e\text{)} \\ &Op_z = \text{V}_{\text{DD}}, \quad z = 0,...,t\text{-}1 && \text{(Refer to } C\text{-}Cal_t \text{ at Fig.11f)} \\ &Sub_t = \overline{\overline{M}.O_t} = \text{GND} && \text{(Refer to } C\text{-}Cal_t \text{ at Fig.11d)} \\ &Add_t = M + O_t + ... + O_0 = \text{V}_{\text{DD}} && \text{(Refer to } C\text{-}Cal_t \text{ at Fig.11e)} \\ &Op_t = \overline{sub_t.add_t} = \text{V}_{\text{DD}} && \text{(Refer to } C\text{-}Cal_t \text{ at Fig.11f)} \end{aligned} \quad (4)$$

As shown in Eq. (4), all LSB blocks collaborate to generate the updated reference current $2^t\times I_{ref}$, used to calibrate BCS_t, $0\le t\le 9$. During this process, all MSB blocks remain disconnected from the Addition and Subtraction Rails. Their M_{opz}, $(0\le z\le t\text{-}1)$ remain ON to deplete excess current and prevent the BCS blocks' transistors from entering the triode region.

2- 4- Fine Calibration Control Signal Generator

Fig. 10 illustrates the Fine Calibration Control Signal Generator (FCCSG) block, which includes the Fine Calibration Digital Core (FCDC), Fine Calibration Thermometer Coder (FCTC), and five Nano Time Interval Generator (NTIG) sub-blocks. The FCDC comprises a 6-bit Fine Sequence Counter (FSC) and a 6×64 Decoder.

At the beginning of the K^{th} fine calibration phase ($C\text{-}Cal_k$ is high, as shown in Fig. 11b), the compensation current is insufficient. The *Q-Comp* output from the Voltage Comparator (VC) oscillates while $\overline{Q\text{-}Comp}$ remains high. This drives the JK flip-flop output (*FCM*) to high (*FCM*=1), activating the 2×1 multiplexer's select line. When (*FCM* and $C\text{-}Cal_k$)=1, the *thermo* (*k,j*) values are directly routed through the I_1 input of the multiplexer to the $M_{FCEC}(k,j)$ switches, which inject fine unary currents from the $M_{Fe}(k,j)$ transistors into the BCS_k sub-block. Initially, the 6-bit counter is reset to zero, so *Nano step (k,0)* and *thermo (k,0)* are high, injecting the compensation current $I(k,0)$. As calibration proceeds, additional $M_{FCEC}(k,j)$ switches are activated sequentially by *Nano step (k,j)* signals to achieve the required compensation current.

When $V_{control}$ reaches V_{ref}, *Q-Comp* becomes high, and the $\overline{Q\text{-}Comp}$ oscillation starts, switching the JK flip-flop output to low (*FCM*=0). This deactivates the 2×1 multiplexer's select line, setting (*FCM* and $C\text{-}Cal_k$)=0. The thermometer, *thermo* (*k,j*), values are latched in the NTIG sub-block, then the latch outputs are connected directly through the I_0 input of the multiplexer gates to the $M_{FCEC}(k,j)$ switches. These values are preserved during the normal operation phase.

The FSC sub-block's *Reset* input (Fig. 10) is triggered by the Add_4 signal, deactivating the 6-bit counter during coarse calibration of the 5-LSB blocks. This reduces overall power consumption. After calibration, all $M_{sub\,t}$ and $M_{add\,t}$ transistors turn OFF, while $M_{op\,t}$ transistors turn ON, enabling normal DAC operation. During normal operation, the input data latched by CLK_n (8 nSec) controls the differential structure, directing the current to the appropriate load.

To minimize power consumption during calibration (see Eq. (5)), CLK_n is masked with *M*, and the calibrated current is directed to R_L regardless of input data. The Clock Mask (C/D Mask) sub-block reduces dynamic power dissipation, expressed as:

$$P = \alpha C V_{DD}^{2} f \quad (5)$$

Where the α is the activity factor, *C* is the load capacitance, V_{DD} is the supply voltage and *f* is the sampling frequency.

3- Simulation Results

The static and dynamic characteristics of the proposed current steering DAC were evaluated by applying an overall current error as high as 125 LSB (62.5 µA for an LSB current of 0.5 µA). Although practical error conditions are significantly smaller, this large error was intentionally introduced into the binary current blocks to demonstrate the robustness of the proposed calibration scheme. The simulations were performed using Cadence with TSMC 180nm CMOS technology. The circuit operates with a 1.8V supply voltage, an LSB current of 500 nA, and a sampling frequency of 125 MHz.

Fig. 12 illustrates the ramp transient response (a, b), Differential Non-Linearity (DNL) (c, d), and Integral Non-Linearity (INL) (e, f) before and after calibration. Without calibration, the total output current was 450 µA, as shown in Fig. 12a. The calibration phase, lasting 1 µsec per block, is clearly visible in Fig. 12b. After calibration, the DAC

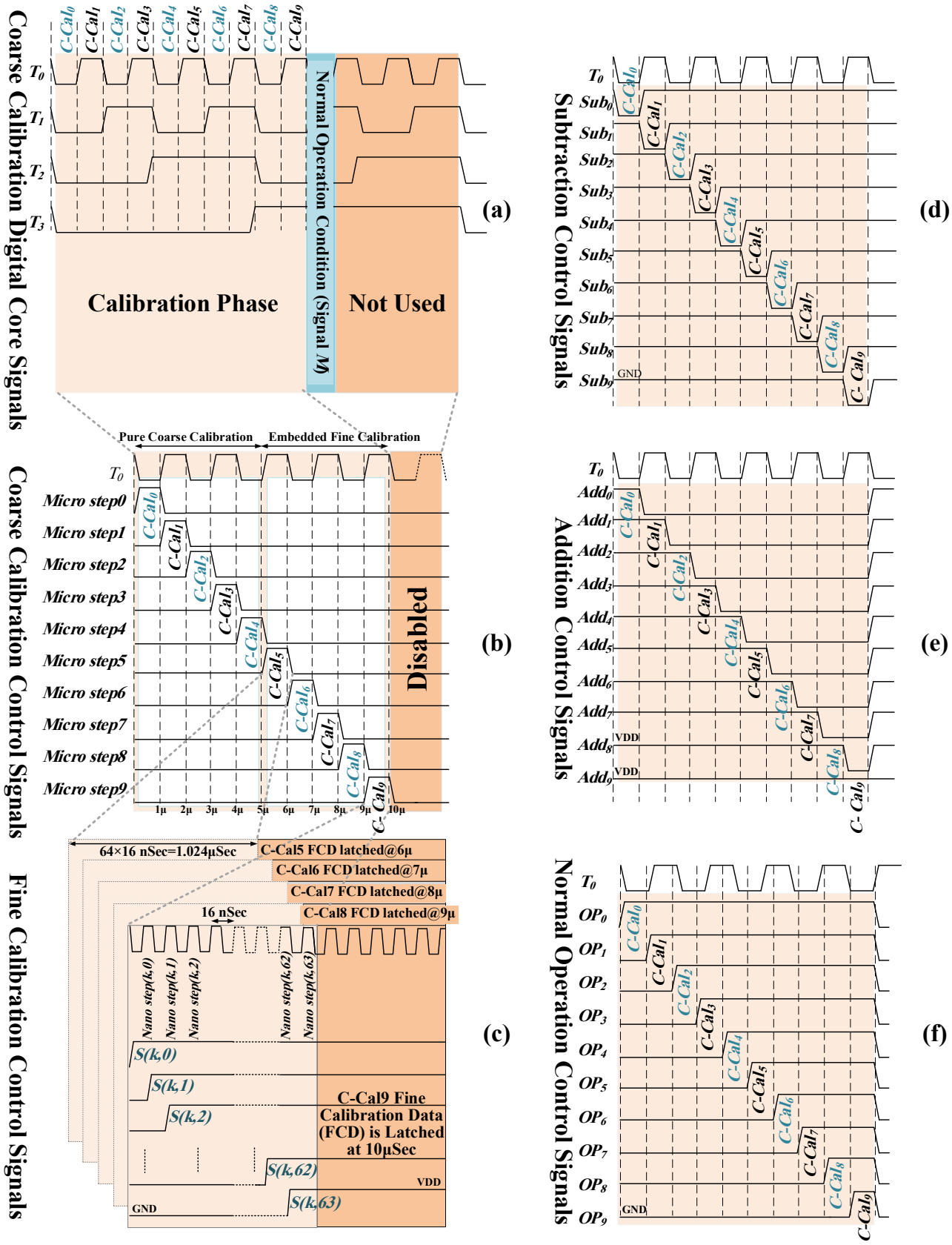

Fig. 8. Addition, Subtraction and Operation signals generated by the Digital Signal Path Control (DSPC) block to control the triple path current steering (TPCS) sub-blocks (a) Calibration and Normal Operation Phase, (b) Subtraction, (c) Addition, and (d) Operation Control Signals.

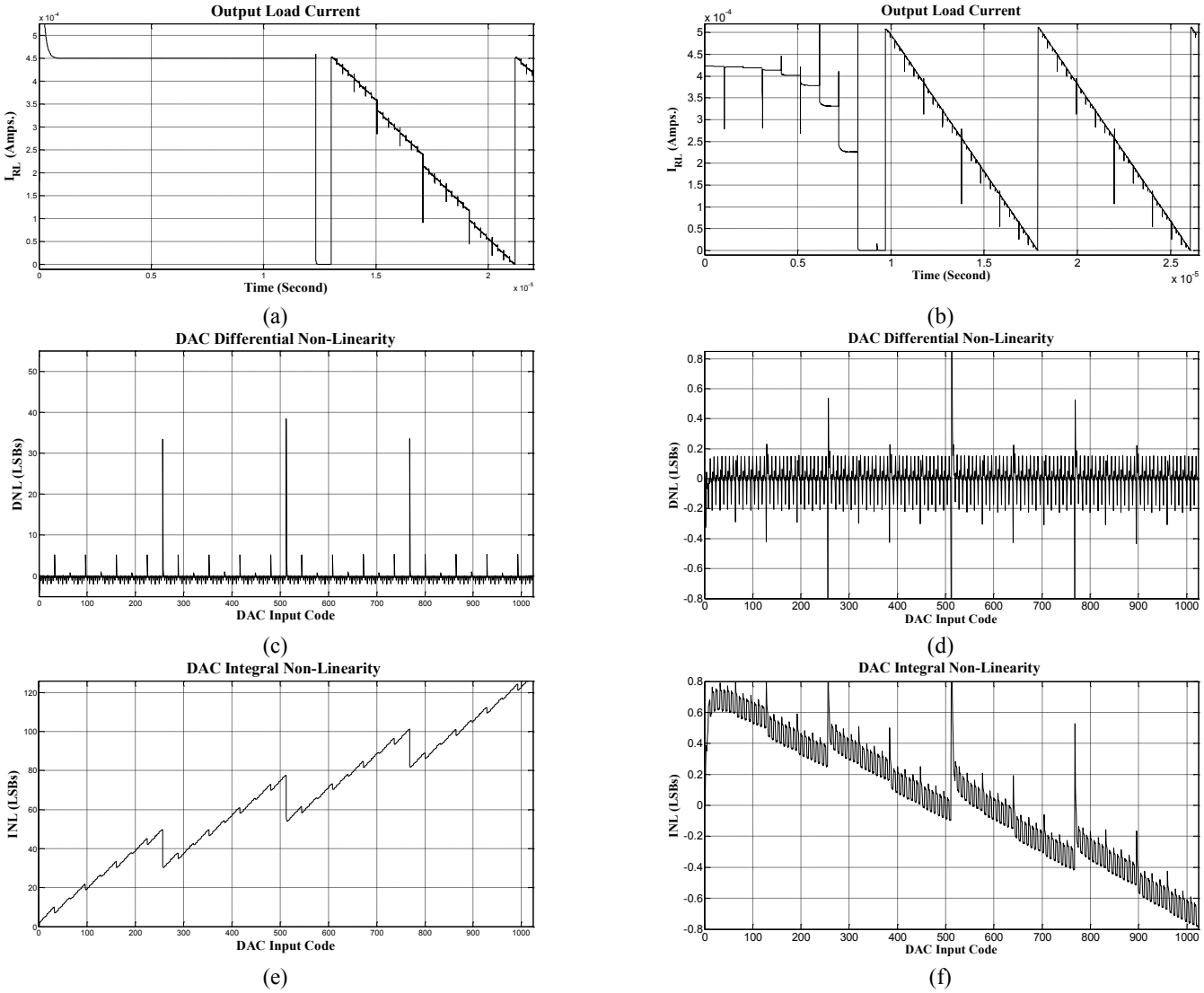

Fig. 12. Ramp transient response (a, b), Differential Non-Linearity (DNL) (c, d), and Integral Non-Linearity (INL) (e, f) before and after calibration, respectively.

transitions to normal operation, achieving a calibrated ramp response (Fig. 12b).

Before calibration, the DAC exhibited significant non-linearities, with DNL values reaching 38 LSB (Fig. 12c) and INL values up to 125 LSB (Fig. 12e). Post-calibration, these values were dramatically reduced to less than ±0.2 LSB for DNL and ±0.8 LSB for INL, as shown in Figs. 12d and 12f, respectively. Fig. 13 shows the sinusoidal transient response and Power Spectrum Density (PSD) of the DAC at 31 MHz for both uncalibrated (a, b) and calibrated (c, d) configurations.

Fig. 14 presents the Spurious Free Dynamic Range (SFDR) curve. Before calibration, the SFDR curve remains nearly constant, fluctuating slightly around 32 dB. After calibration, the SFDR improves significantly, starting at approximately 70.3 dB for low-frequency input signals and decreasing to about 59.7 dB at the Nyquist rate.

The proposed calibration scheme employs a single calibration circuit algorithmically and serially, while also managing dynamic power consumption by masking the high-frequency sampling signal during idle modes. Combined with a low supply voltage of 1.8V and an LSB current of 500 nA, this approach reduces overall power consumption to a remarkably low value of 2.1 mW.

Table 1 provides a comparison of the proposed calibration technique with alternative methods, highlighting its advantages in terms of accuracy, efficiency, and power consumption. Table 2 also lists current steering DAC specifications (SFDR, THD, SNR, SNDR, and ENOB) for several input signal frequencies before and after calibration. It is worth noting that in the proposed paper, the authors have considered worse input current signals to show the effectiveness of the calibration method in diminishing these issues.

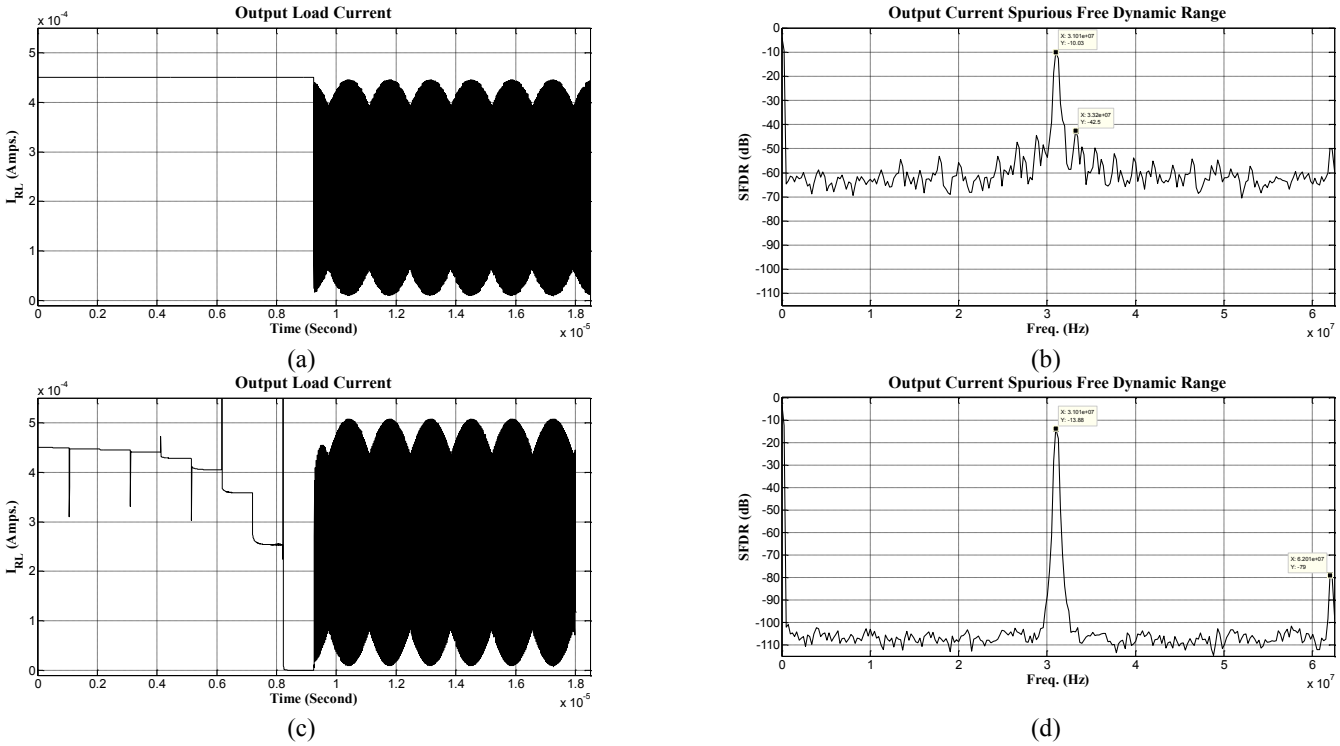

Fig. 13. Sinusoidal transient response and Power Spectrum Density of the digital to analog converter at 31 MHz for un-calibrated (a, b) and calibrated (c, d) structures.

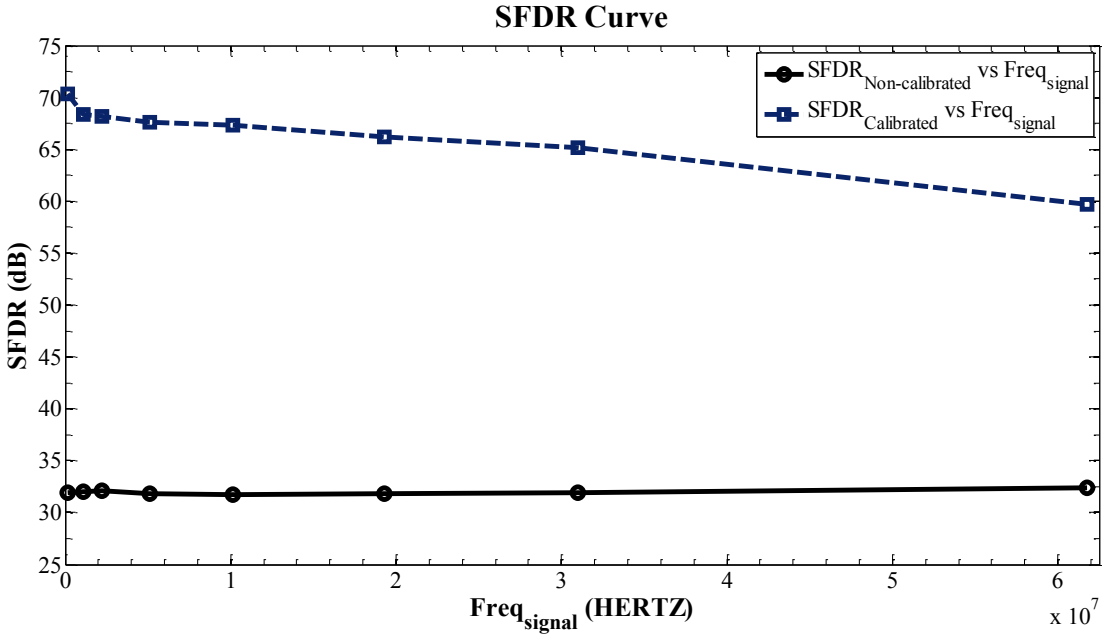

Fig. 14. Spurious Free Dynamic Range (SFDR) curve before and after calibration.

4- Conclusion

A novel calibration technique for binary-weighted Current Steering DACs is presented, driven by the need for simplicity and ultra-low power performance. Despite the structural limitations of such DACs, which often hinder matching accuracy, few existing calibration methods address these issues effectively. This paper introduces an innovative foreground calibration method capable of dynamically, arbitrarily, and repeatedly calibrating the DAC.

The system utilizes two clock frequencies: 1 MHz for calibration and 125 MHz for normal operation. By employing a unique calibration block in an algorithmic fashion, the proposed structure effectively eliminates transistor mismatch errors across all current blocks. A configurable triple-path scheme is implemented to update the reference current by summing the adjusted LSB currents and using this updated reference to calibrate the next higher MSB current.

To validate the effectiveness of the proposed calibration method, an exaggerated current error of 125 LSB was intentionally introduced into the binary current blocks. Simulations for a 10-bit DAC were conducted using Cadence and TSMC 180nm CMOS technology, with a 125 MHz sampling frequency, 1.8V supply voltage, and 500 nA LSB current. The proposed structure demonstrated extremely low power consumption, achieving a remarkable 2.1 mW, making it highly suitable for low-power portable applications.

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