

Studying the Impact of Technology Scaling on the Performance of MOSFET Devices Using Semi-Empirical Modeling through the Inversion Coefficient

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ABSTRACT: For six decades, integrated circuit design and manufacturing have fueled information technology's explosive growth, powering modern computing and advancing contemporary civilization. Advancements in this industry are primarily driven by the shrinking of technology and the reduction of transistor channel length in metal oxide semiconductor devices. This paper examines the impact of these factors on the characteristics and performance trade-offs of metal oxide semiconductor devices, focusing on the inversion coefficient as a key design parameter across all inversion regions (Weak Inversion, Moderate Inversion, and Strong Inversion). The performance trade-offs, analyzed in terms of inversion coefficient in 90nm and 180nm processes, encompass sizing relationships, DC bias and small signal parameters, gain and bandwidth, gate-referred thermal and flicker noise, DC mismatch, gate-source leakage and figure of merit for low-power radio frequency designs. Graphically displaying performance trends against inversion coefficient across two fabrication technologies allows for selection of desired trade-offs as the process is shrunk. Finally, an operating plane for metal oxide semiconductor devices is presented, enabling the selection of appropriate bias points to optimize device performance within the desired circuit as technology scales down.

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1- Introduction

As shown in Fig. 1, the history of electronics is marked by three key components: vacuum tubes, bipolar junction transistors, and MOSFETs. While vacuum tubes and BJTs significantly advanced computing, the advent of MOSFETs, particularly CMOS technology, has fueled the rapid growth of information technology and driven modern civilization for the last six decades [1]. To meet demands for increased speed, power efficiency, and density in integrated circuits, MOSFET channel lengths have shrunk below 20nm, a trend predicted by Gordon Moore in his 1965 Moore's Law. The key advantage of MOSFET technology for VLSI circuits is that scaling down its physical size improves crucial metrics like cost, performance, and power consumption. Furthermore, CMOS technology's field-effect nature and extremely low leakage power make it highly desirable for low-power applications. However, scaling down MOSFET technology has presented challenges. As device sizes has reached micron and submicron scales, CMOS technology faces challenges such as short-channel effects (SCEs) [2].

Before the 21st century, CMOS technology refinement focused on reducing gate oxide thickness and engineering source, drain, and channel impurities. Over the past two

decades, innovations in materials and architectures like SC¹, HKMG², SOI³, and FinFETs⁴ have aimed to suppress SCEs and other undesirable effects [3–10]. In advanced manufacturing, technology-driven reductions in supply voltage have shifted transistor operating points towards the moderate inversion and weak inversion regions [11]. Consequently, the older MOSFET drain current equations in Level 1 and Level 3 models are unsuitable for modern submicron technologies and lead to inaccurate performance evaluations [12]. On the other hand, designing analog and RF circuits presents a significant challenge in balancing various factors such as power, linearity, noise, gain, supply voltage, and bandwidth. Razavi has illustrated these factors as the vertices of a hexagon [13]. In traditional manufacturing technologies, the effective gate-source voltage, $V_{EFF} = V_{GS} - V_T$, was a key design variable. However, with advancements in technology and the reduction of gate lengths in MOSFET devices in recent years, as well as the shift of their bias points into weak and moderate inversion regions, V_{EFF} is no longer regarded as a suitable design parameter. This is due to its nonlinear relationship with drain current [14, 15].

In 1994, Vittoz published a paper titled "Low Power Techniques," in which he defined the concept of the inversion

- 1 Strained Channel
- 2 High-dielectric-constant (k) metal gate
- 3 Silicon on Insulator
- 4 Fin Field-Effect Transistors

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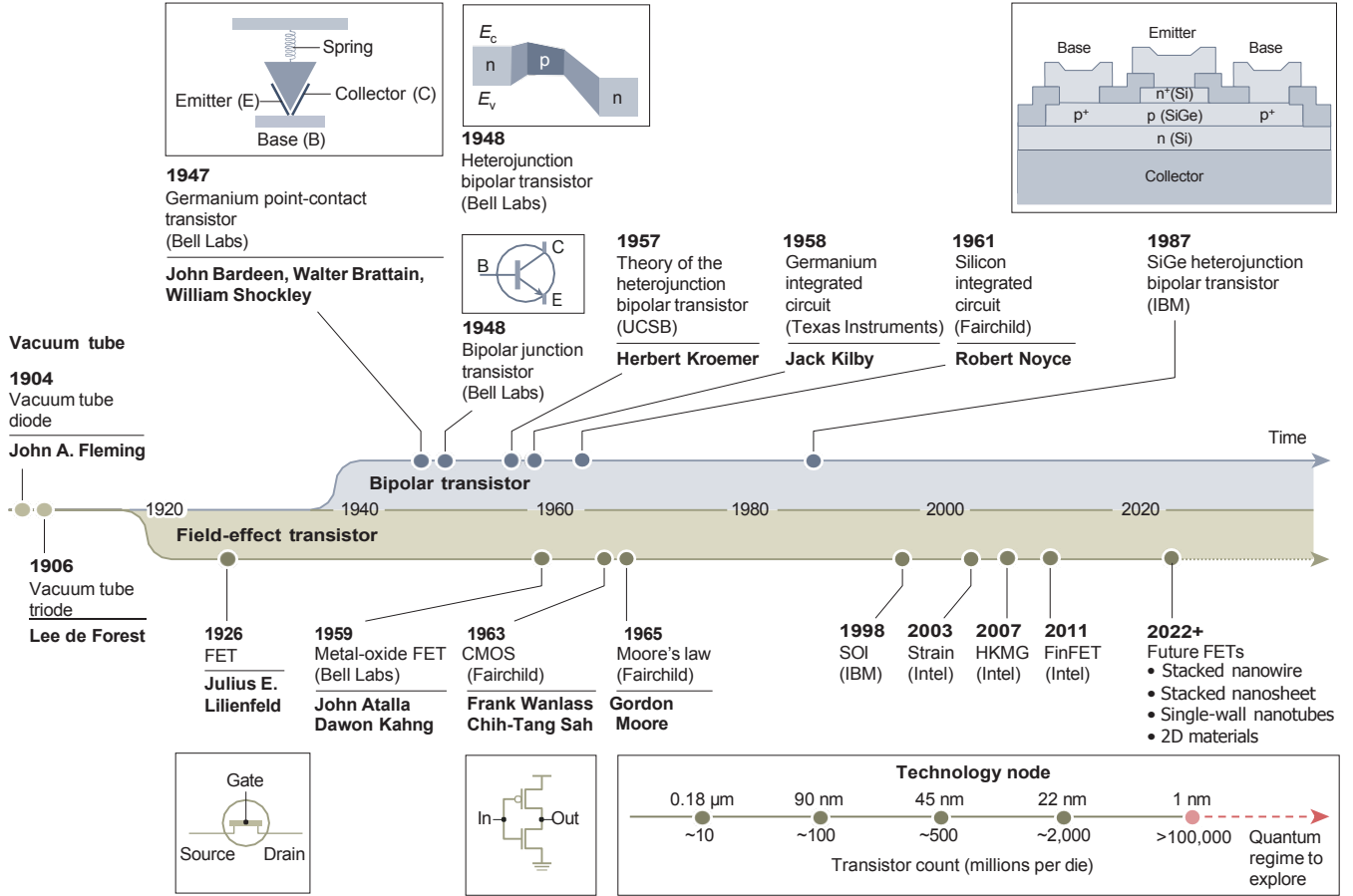


Fig. 1. Transistor technology timeline. The shift from vacuum tubes to BJTs and then MOSFETs was largely driven by the need for reduced power consumption [1].

coefficient (IC) [16]. IC is the normalized value of the drain current relative to the characteristic current of the MOSFET device [17]:

$$IC = \frac{I_D}{I_{spec}} = \frac{I_D}{I_0(W/L)}, \quad I_0 = 2n\mu C_{ox}U_T^2 \quad (1)$$

where L and W are the gate length and width of a transistor, n is the body factor, μ is the mobility, C_{ox} is the oxide capacitance per unit area and $U_T = kT/q = 25.8mV$ is the thermodynamic voltage at standard room temperature. The value of the IC indicates the level of inversion in a transistor, independent of both the technology used and the size of the transistor:

- $IC < 0.1$, Weak Inversion (WI),
- $0.1 < IC < 10$, Moderate Inversion (MI),
- $IC > 10$, Strong Inversion (SI),

Modeling MOS devices using the IC in the WI and MI regions is more suitable due to the linear relationship

between the IC and the drain current. Additionally, IC allows for the interpretation of important parameters of the MOS transistor, such as sizing relationships, DC bias and small signal parameters, gain and bandwidth, gate-referred thermal and flicker noise, DC mismatch, gate-source leakage, and figure of merit for low-power RF designs [18]. Therefore, by varying the IC of MOSFET devices within a circuit, it is possible to identify their optimal operating points.

Selecting a design model is the initial step in designing analog and RF circuits. Among these, the EKV model stands out for its simplicity and reliability in predicting the complex physics of modern submicron MOSFET devices while also supporting low-power designs. In 1995, C. Enz, F. Krummenacher, and E. A. Vittoz developed the EKV model for MOS transistors [19,20]. It is a physics-based semi-empirical model that uses appropriate assumptions and approximations to keep the equations simple for hand calculations. The EKV model defines the drain current of a MOS transistor as continuous from the weak inversion (WI) to the strong inversion (SI) region:

$$I_D(WI - SI) = 2n\mu C_{ox} U_T^2 \left(\frac{W}{L} \right) \left[\ln \left(1 + e^{\frac{V_{GS} - V_T}{2nU_T}} \right) \right]^2 \quad (2)$$

To account for small geometry effects of MOS devices, such as velocity saturation and vertical field mobility reduction (VFMR), μ can be replaced with Eq. (3), where θ is the carrier mobility reduction coefficient due to the vertical field. E_{CRIT} is the horizontal critical electric field at velocity saturation, and α is the power coefficient of velocity saturation.

$$\frac{\mu_0}{[1 + \theta(V_{GS} - V_T)] \left[1 + \left(\frac{V_{GS} - V_T}{LE_{CRIT}} \right)^\alpha \right]^{\frac{1}{\alpha}}} \quad (3)$$

Recently, severally studies have highlighted the advantages of using the inversion coefficient in the design of analog and RF circuits. For instance, Sansen proposed a method for designing low-power amplifier blocks and optimizing components to achieve zero distortion using the EKV/BSIM6 models [21,22]. Additionally, in another study, the linearity indices A1dB and AIP3 were analyzed in single-stage and cascode differential amplifiers based on the EKV model and its primary parameter, the inversion coefficient [23].

In this paper, the performance variations of MOSFET devices, including sizing relationships, DC bias and small signal parameters, gain and bandwidth, gate-referred thermal

and flicker noise, DC mismatch, gate-source leakage, and figure of merit for low-power RF designs, are graphically compared in terms of inversion coefficient (IC) in two processes of 90nm and 180nm. In the following, an operating plane is introduced that shows the performance trade-offs versus IC and the desired manufacturing process (technology shrinking) at a constant bias current. This operating plane displays how MOSFET device performance changes with advancements in technology.

The paper is structured as follows: Section 2 summarizes the key parameters of the EKV model for the 90nm and 180nm processes. Section 3 graphically compares the performance characteristics of the MOS device in terms of IC for both processes and briefly explains how technology shrinking affects MOSFET performance from weak to strong inversion regions. Finally, Section 4 introduces the MOSFET operating plane to illustrate performance trade-offs related to the inversion coefficient and the desired fabrication.

2- Process Parameters

The EKV model requires almost 70 parameters to describe the device and its physical phenomena, even though it has fewer parameters and equations than the more complex BSIM model [24]. One method for extracting EKV parameters involves converting BSIM parameters using the Levenberg-Marquardt algorithm for 0.18 μm CMOS technology [25]. This paper develops MOS trade-off performance using key design parameters of the EKV model and five optional parameters, as shown in Tables 1 and 2 for 90 nm and 180 nm technologies, respectively.

Table 1. Key process parameters of the EKV model for nMOS and pMOS transistors in 90nm CMOS technology.

Parameter	Description	Value for nMOS	Value for pMOS	Unit
t_{ox}	Oxide Thickness	2.33	2.5	nm
μ_0	Low Field Mobility	454	95	$\mu\text{A}/\text{V}^2$
Y	Body Effect Factor	0.32	0.16	$\text{V}^{1/2}$
V_{sat}	Saturation Velocity	114000	120000	m/s
α	Velocity Saturation Transition Exponent	1.15	1.15	--
n	Slope Factor	1.3	1.3	--
V_{T0}	Threshold Voltage	0.375	0.17	V
θ	Mobility Reduction Factor	0.51	0.48	V^{-1}
β	Exponent for Velocity Saturation & VFMR Effects	0.8	0.9	--
DL	Lateral Diffusion at Length	0.005	0.005	μm
DW	Lateral Diffusion at Width	0.012	0.01	μm
AF	Flicker Noise Slope	0.85	1.09	--
ϕ_F	Half of the Fermi Potential	0.428	0.42	V
L_{min}	Minimum Channel Length	0.09	0.09	μm
TCV	Threshold Voltage Temperature Coefficient	0.0003	-0005	V/C
BEX	Mobility Temperature exponent	-1.2	-1.1	--
UCEX	Velocity Saturation, Critical Electric Field Temperature exponent	1.5	3.5	--
Optional user design inputs				
f	Operation Frequency	1	1	Hz
V_{DD}	Supply Voltage	--	--	V
V_{SB}	Source-Body Voltage	--	--	V
V_{DS}	Drain-Source Voltage	--	--	V
T	Temperature	300	300	K

Table 2. Key process parameters of the EKV model for nMOS and pMOS transistors in 180nm CMOS technology.

Parameter	Description	Value for nMOS	Value for pMOS	Unit
t_{ox}	Oxide Thickness	4.1	4.1	nm
μ_0	Low Field Mobility	422	89.2	$\mu A/V^2$
γ	Body Effect Factor	0.56	0.61	$V^{1/2}$
V_{sat}	Saturation Velocity	90659.09	151306.8	m/s
α	Velocity Saturation Transition Exponent	1.3	1.3	--
n	Slope Factor	1.35	1.3	--
V_{T0}	Threshold Voltage	0.42	0.42	V
θ	Mobility Reduction Factor	0.28	0.35	V^{-1}
β	Exponent for Velocity Saturation & VFMR Effects	0.8	0.9	--
DL	Lateral Diffusion at Length	0.028	0.051	μm
DW	Lateral Diffusion at Width	0	0	μm
AF	Flicker Noise Slope	0.85	1.05	--
ϕ_F	Half of the Fermi Potential	0.425	0.425	V
L_{min}	Minimum Channel Length	0.18	0.18	μm
TCV	Threshold Voltage Temperature Coefficient	0.0006	0.0006	V/C
BEX	Mobility Temperature exponent	-1.5	-1.5	--
UCEX	Velocity Saturation, Critical Electric Field Temperature exponent	0.8	3.5	--
Optional user design inputs				
f	Operation Frequency	1	1	Hz
V_{DD}	Supply Voltage	--	--	V
V_{SB}	Source-Body Voltage	--	--	V
V_{DS}	Drain-Source Voltage	--	--	V
T	Temperature	300	300	K

3- Comparison of MOS device performance versus inversion coefficient in the 90nm and 180nm processes.

This section analyzes and compares the performance trade-offs of the MOSFET device, including sizing relationships, DC bias and small signal parameters, gain and bandwidth, gate-referred thermal and flicker noise, DC mismatch, gate-source leakage, and figure of merit for low-power RF designs, using process parameters from Tables 1 and 2 and MOS characteristics derived from the EKV model in Table 3. The analysis focuses on the two technologies, 90nm and 180nm, using MATLAB software. Given that the trends for nMOS and pMOS transistors regarding IC are similar and mainly differ in parameters like n and μ , we focus on the nMOS device's behavior in relation to the inversion coefficient in both technologies. In all simulations, the drain current is kept at $100\mu A$ and the channel lengths at 90nm and 180nm, while the IC value is swept from 0.01 (deep weak inversion) to 100 (deep strong inversion).

3- 1- Sizing parameters

Fig. 2 presents the aspect ratio (W/L) and gate area (WL) of an nMOS device as a function of the inversion coefficient for 90nm and 180nm CMOS processes at a drain current of $100\mu A$. The figure clearly shows that as technology shrinks, the aspect ratio, channel width, and gate area decrease.

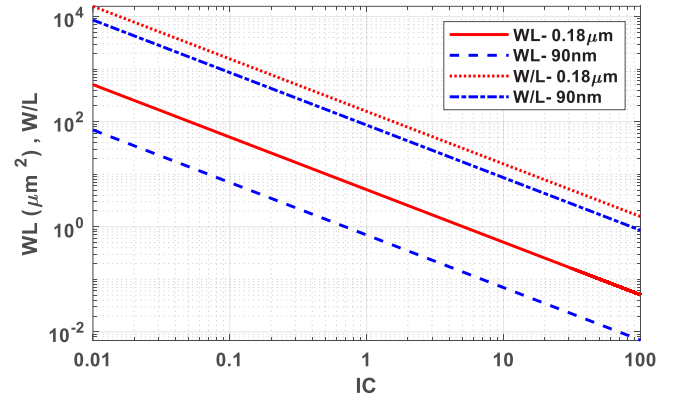


Fig. 2. Aspect ratio, W/L, and gate area, WL, of an nMOS device versus the inversion coefficient for 90nm and 180nm CMOS processes at a drain current of $100\mu A$, with L equal to 90nm and 180nm.

3- 2- DC bias parameters

Fig. 3a illustrates the changes in $V_{EFF} = V_{GS} - V_T$, effective gate-source voltage, and $V_{DS_{sat}}$, drain-source saturation voltage, of the nMOS device versus the inversion coefficient across two CMOS processes, 90nm and 180nm CMOS processes, at a drain current of $100\mu A$. The data shows that while V_{EFF} remains relatively stable in the

Table 3. MOS device characteristics derived from the EKV model.

Specification	Equation	Description	Unit
Sizing Relationships	$W = \left(\frac{L}{IC}\right) \cdot \left(\frac{I_D}{I_0}\right)$	Width	μm
	$WL = \left(\frac{L^2}{IC}\right) \left(\frac{I_D}{I_0}\right)$	Gate Area	μm^2
	$\frac{W}{L} = \left(\frac{1}{IC}\right) \left(\frac{I_D}{I_0}\right)$	Shape Factor	--
DC Bias Parameters	$V_{EFF} = 2nU_T \ln(e^{\sqrt{A}} - 1)$	Effective Gate-Source Voltage	V
	$V_{DSsat} = 2U_T \sqrt{IC} + 0.25 + 3U_T$	Drain-Source Saturation Voltage	V
Small Signal Parameters	$\frac{g_m}{I_D} = \frac{1}{nU_T(\sqrt{B+0.25} + 0.5)}$	Transconductance Efficiency	V^{-1}
	$\frac{g_{ds}}{I_D} = \frac{1}{V_A + V_{DS}}$	Drain-Source Conductance Efficiency	V^{-1}
	$g_m = \left(\frac{g_m}{I_D}\right) \cdot I_D$	Transconductance	μS
	$g_{ds} = \left(\frac{g_{ds}}{I_D}\right) \cdot I_D$	Drain-Source Conductance	μS
	$g_{mb} = \eta \cdot g_m$	Body Effect Transconductance	μS
	$r_{ds} = (g_{ds})^{-1}$	Drain-Source resistance	$K\Omega$
	$A_{1dB}(WI) = 1.22(nU_T)$	Input 1dB Compression Voltage for a Differential Pair in WI Region	V
	$A_{1dB}(SI) = 1.81(nU_T\sqrt{B})$	Input 1dB Compression Voltage for a Differential Pair in SI Region	V
Gain & Bandwidth Relationships	$V_A = V_A(CLM) \parallel V_A(DIBL)$	Early Voltage	V
	$A_{Vi} = \frac{V_A}{nU_T(\sqrt{B+0.25} + 0.5)}$	Intrinsic Voltage Gain	--
	$f_{Ti} = \left(\frac{IC}{\sqrt{B+0.25} + 0.5}\right) \left(\frac{\mu U_T}{\pi(C_{gs1} + C_{gbi})L^2}\right)$	Intrinsic Bandwidth	GHZ
	$f_T = \frac{g_m}{2\pi(C_{gs1} + C_{gbi})}$	Bandwidth	GHZ
Gate Referred Thermal & Flicker Noise	$S_{VG} = 4KT(n\Gamma\sqrt{B+0.25} + 0.5) \left(\frac{nU_T}{I_D}\right)$	Gate Referred Thermal Noise Voltage PSD1	nV^2/HZ
	$\sqrt{S_{VG}} = \sqrt{4KT(n\Gamma\sqrt{B+0.25} + 0.5) \left(\frac{nU_T}{I_D}\right)}$	Square Root of Gate Referred Thermal Noise Voltage PSD	nV/\sqrt{HZ}
	$S_{VG}(f) = \left(\frac{IC}{L^2}\right) \left(\frac{I_0}{I_D}\right) \frac{K_F}{C_{OX}^2 f^{AF}}$	Gate Referred Flicker Noise Voltage PSD	nV^2/HZ
	$\sqrt{S_{VG}(f)} = \sqrt{\left(\frac{IC}{L^2}\right) \left(\frac{I_0}{I_D}\right) \frac{K_F}{C_{OX}^2 f^{AF}}}$	Square Root of Gate Referred Flicker Noise Voltage PSD	nV/\sqrt{HZ}
	$f_c = \left[\frac{2\pi K_F}{4KT C_{OX}} \left(\frac{C_{gs1} + C_{gbi}}{n\Gamma}\right)\right]^{\frac{1}{AF}}$	Corner Frequency	GHZ
Local Area DC Mismatch	$\Delta V_T = AV_{T0} \left(1 + \frac{V_{SB}}{2\phi_0}\right) \left(\frac{\sqrt{IC}}{L} \cdot \sqrt{\frac{I_0}{I_D}}\right)$	Threshold Voltage Mismatch	mV
	$\frac{\Delta K_P}{K_P} = A_{KP} \left(\frac{\sqrt{IC}}{L} \cdot \sqrt{\frac{I_0}{I_D}}\right)$	Relative Transconductance Mismatch	--
	$\Delta V_{GS} = \left(\frac{\sqrt{IC}}{L} \cdot \sqrt{\frac{I_0}{I_D}}\right) \cdot \sqrt{AV_T^2 + [A_{KP} nU_T(\sqrt{B+0.25} + 0.5)]^2}$	Gate-Source Voltage Mismatch	mV
	$\frac{\Delta I_D}{I_D} = \left(\frac{\sqrt{IC}}{L} \cdot \sqrt{\frac{I_0}{I_D}}\right) \cdot \sqrt{\left(\frac{AV_T}{nU_T(\sqrt{B+0.25} + 0.5)}\right)^2 + A_{KP}^2}$	Relative Drain Current Mismatch	--
Gate-Source Leakage Current	$I_{(GS)L} = \left(\frac{L^2}{IC}\right) \left(\frac{I_D}{I_0}\right) K_{GA} \left[nU_T \ln\left(1 + e^{\frac{V_{EFF}}{nU_T}}\right)\right] V_{GS} e^{K_{GB} \cdot V_{GS}}$	Gate-Source Leakage Current	μA
Figure of Merits	$\left(\frac{g_m}{I_D} \cdot f_{Ti}\right)$	Low Power RF Design Figure of Merit	$V^{-1}GHZ$
	$= \left(\frac{1}{nU_T(\sqrt{B+0.25} + 0.5)}\right) \left(\frac{IC}{\sqrt{B+0.25} + 0.5}\right) \left(\frac{\mu U_T}{\pi(C_{gs1} + C_{gbi})L^2}\right)$		
	$(A_{Vi} \cdot f_{Ti})$	Intrinsic Gain Bandwidth	GHZ
$K = 1.380649 * 10^{-23}$ is Boltzmann Constant.			

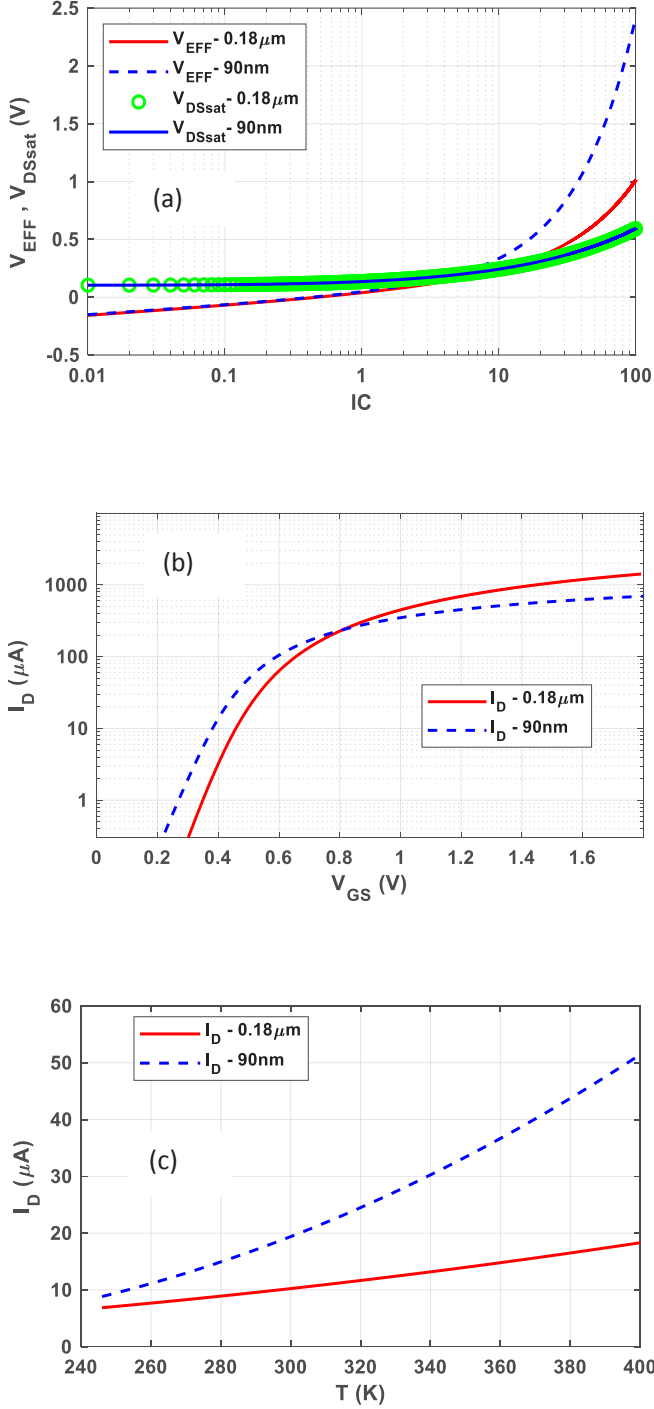


Fig. 3. (a) Effective gate-source voltage, V_{EFF} , and drain-source saturation voltage, V_{DSsat} , of an nMOS device versus the inversion coefficient for 90nm and 180nm CMOS processes at a drain current of 100 μA , (b) Drain current, I_D , versus gate-source voltage, V_{GS} , and (c) Drain current, I_D , versus temperature, T , for an nMOS device in both 90nm and 180nm CMOS processes at a fixed inversion coefficient (IC=1).

WI and MI regions, there is a significant increase in the SI region for the 90nm process due to velocity saturation caused by small geometry effects. The relationship $V_{DSsat} = 2U_T \sqrt{IC + 0.25} + 3U_T$ indicates that its value is mostly invariant with technology shrinking [26]. Typically, MOS devices operate in the saturation region, where $V_{DS} > V_{DSsat}$. Fig. 3b shows the trend of I_D , drain current, of the nMOS device versus the gate-source voltage, V_{GS} , (equations 1 and 2) across two CMOS processes, 90nm and 180nm CMOS processes. While both processes exhibit similar trends at lower V_{GS} , the current drop is more significant at higher V_{GS} due to the velocity saturation caused by small geometry effects in the 90nm process. Temperature influences many of the drain current parameters of the MOS device, including $V_{T0}(T) = V_{T0} + TCV \cdot (T - T_{NOM})$, $\mu_0(T) = \mu_0 \cdot (T/T_{NOM})^{BEX}$, $E_{CRIT}(T) = E_{CRIT} \cdot (T/T_{NOM})^{UCEX}$ and $U_T(T) = KT/q = 25.85mV(T/300K)$. TCV, BEX and UCEX are the process parameters listed in Tables 1 and 2. T_{NOM} is the nominal temperature (27 $^{\circ}C$). Fig. 3c illustrates the changes in I_D , drain current, of the nMOS device versus temperature in 90nm and 180nm CMOS processes. Temperature ranges are defined from -33 $^{\circ}C$ to 127 $^{\circ}C$ (240K to 400K). Drain current variations in the specified temperature range are more significant for the 90nm CMOS process due to the velocity saturation caused by small geometry effects.

3-3- Small signal parameters

Fig. 4 shows the trend of g_m/I_D , transconductance efficiency, of the nMOS device versus the inversion coefficient in two CMOS processes, 90nm and 180nm. The figure indicates that while g_m/I_D remains nearly constant in weak inversion, it decreases in strong inversion due to velocity saturation caused by small geometry effects.

Fig. 5 displays the trends of g_m , transconductance, g_{mb} , body-effect transconductance, and g_{ds} , drain-source

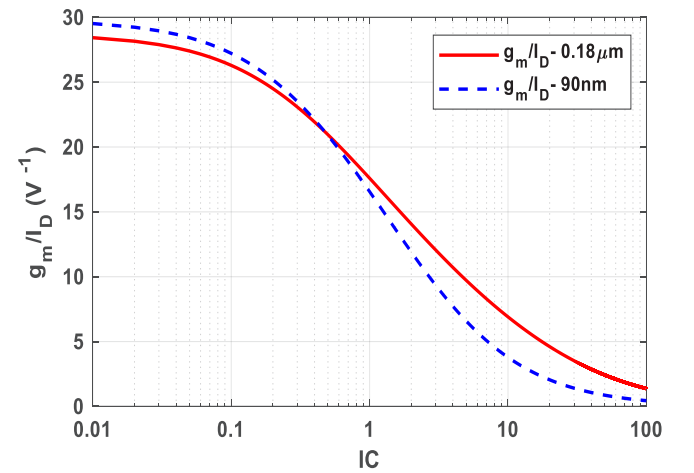


Fig. 4. Transconductance efficiency, g_m/I_D , of an nMOS device versus the inversion coefficient for 90nm and 180nm CMOS processes.

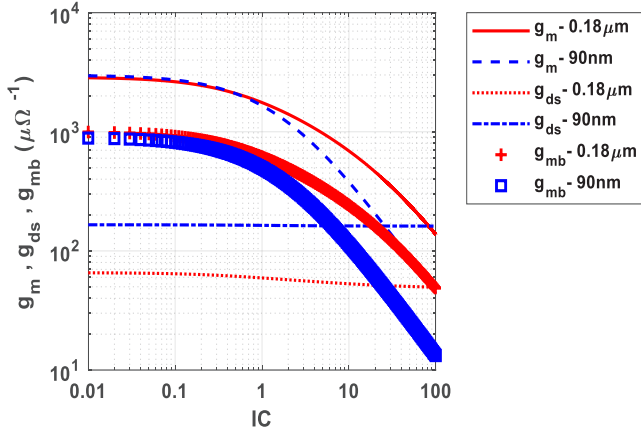


Fig. 5. transconductance, g_m , body-effect transconductance, g_{mb} , and drain-source conductance, g_{ds} , of an nMOS device versus the inversion coefficient for 90nm and 180nm CMOS processes at a drain current of 100 μ A.

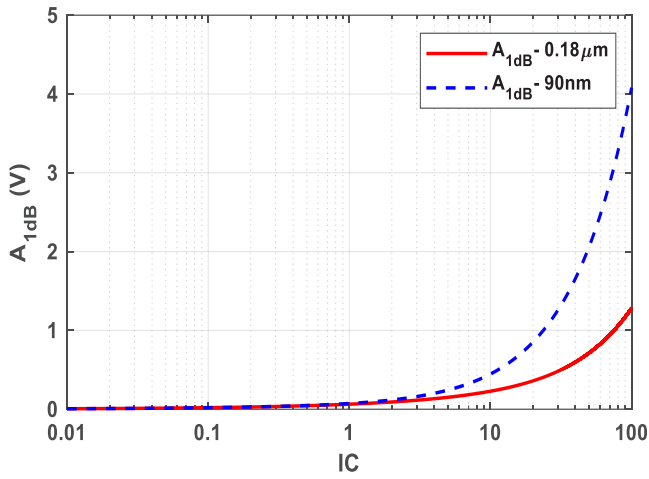


Fig. 6. input 1dB compression voltage, A_{1dB} , of an nMOS device versus the inversion coefficient for 90nm and 180nm CMOS processes at a drain current of 100 μ A.

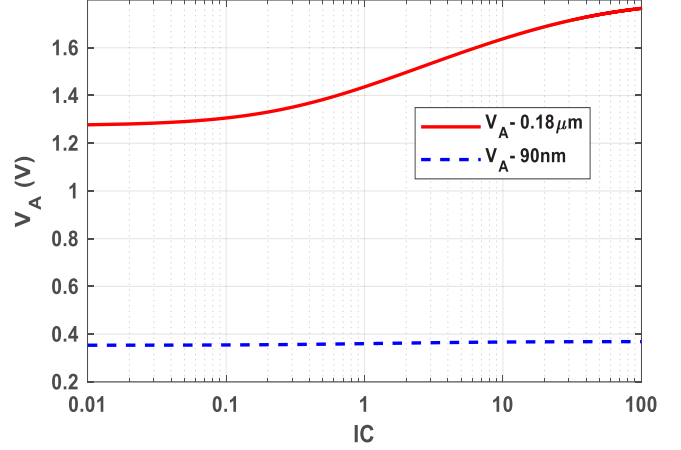


Fig. 7. Intrinsic voltage gain, A_{Vi} , of an nMOS device versus the inversion coefficient for 90nm and 180nm CMOS processes at a drain current of 100 μ A and $V_{DS}=0.25$ V.

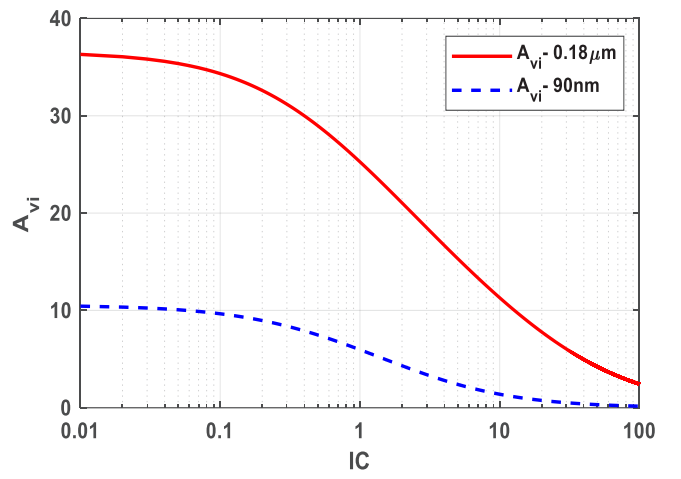


Fig. 8. Intrinsic voltage gain, A_{Vi} , of an nMOS device versus the inversion coefficient for 90nm and 180nm CMOS processes at a drain current of 100 μ A and $V_{DS}=0.25$ V.

conductance, of the nMOS device versus the inversion coefficient in 90nm and 180nm CMOS processes. The data shows that while g_m , g_{mb} , and g_{ds} remain nearly constant in weak inversion, they decrease in strong inversion due to velocity saturation caused by small geometry effects.

Fig. 6 illustrates the changes in A_{1dB} , input 1dB compression voltage, of the nMOS device versus the inversion coefficient in the same CMOS processes. As shown, the shrinking of technology improves linear performance, as A_{1dB} has an inverse relationship with g_m / I_D .

3- 4- Gain and Bandwidth parameters

Fig. 7 shows the trend of V_A , early voltage, of the nMOS device versus the inversion coefficient in 90nm and 180nm CMOS processes. The figure indicates that as technology shrinks, V_A decreases due to the reduction in channel length and r_{ds} . Fig. 8 depicts the changes in A_{Vi} , intrinsic voltage gain, of the nMOS device based on IC in the same processes. Here, A_{Vi} sharply decreases with technology shrinking due to the decline in V_A and g_m / I_D . Fig. 9 illustrates the trends of f_{Ti} , intrinsic bandwidth, f_T , bandwidth, and

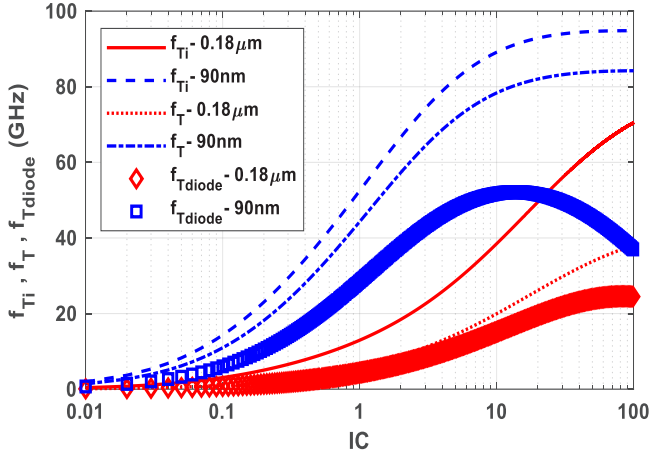


Fig. 9. Intrinsic bandwidth, f_{Ti} , bandwidth, f_T , and diode connected bandwidth, f_{Tdiode} , of an nMOS device versus the inversion coefficient for 90nm and 180nm CMOS processes.

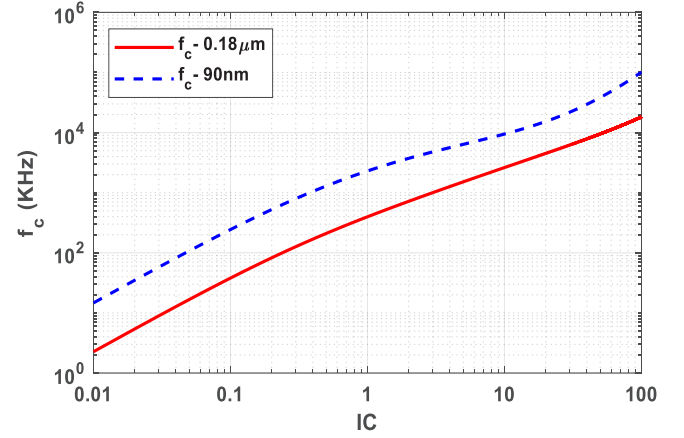


Fig. 11. Flicker noise corner frequency, f_c , of an nMOS device versus the inversion coefficient for 90nm and 180nm CMOS processes at a drain current of 100 μA .

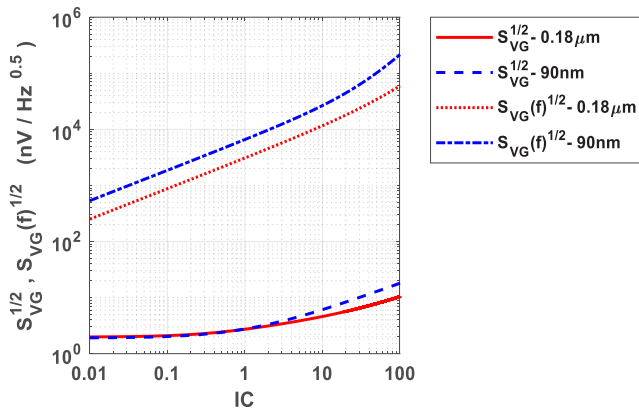


Fig. 10. Gate-referred thermal noise voltage density, $S_{VG}^{1/2}$, and gate-referred flicker noise voltage density, $S_{VG}^{1/2}(f)$, of an nMOS device versus the inversion coefficient for 90nm and 180nm CMOS processes at a drain current of 100 μA .

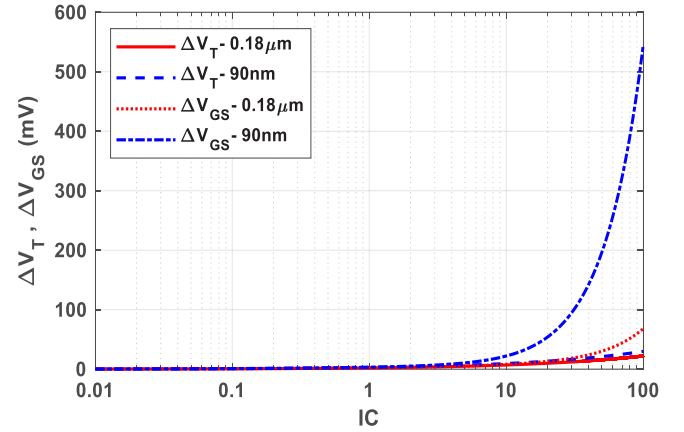


Fig. 12. Threshold voltage mismatch, ΔV_T , and gate-source voltage mismatch, ΔV_{GS} , of an nMOS device versus the inversion coefficient for 90nm and 180nm CMOS processes at a drain current of 100 μA .

f_{Tdiode} , diode-connected bandwidth, against the inversion coefficient. It shows that as technology improves, f_{Ti} , f_T , and f_{Tdiode} increase due to the decrease in L . However, in the 90nm process, the greater velocity saturation due to the device's small geometry effects results in a smaller decrease in these values across inversion coefficients. Thus, it can be concluded that IC_{CRIT} in the 90nm process is smaller than in the 180nm process.

3- 5- Gate-referred Thermal and Flicker noise Parameters

Fig. 10 presents the trends in the gate-referred thermal noise voltage density, $S_{VG}^{1/2}$, and the gate-referred flicker noise voltage density, $S_{VG}^{1/2}(f)$, of the nMOS device versus the

inversion coefficient in 90nm and 180nm CMOS processes at a drain current of 100 μA . The figure shows that $S_{VG}^{1/2}$ remains relatively stable in the WI and MI regions, but increases in the SI region due to velocity saturation caused by small geometry effects. Similarly, $S_{VG}^{1/2}(f)$ (also increases with technology shrinking. Fig. 11 displays the trend in f_c , flicker noise corner frequency, of the nMOS device versus the inversion coefficient in the same CMOS processes and drain current. The trend of f_c changes parallels that of thermal and flicker noise, increasing as technology advances.

3- 6- Local Area DC Mismatch Parameters

Fig. 12 shows the trends in threshold voltage mismatch, ΔV_T , and gate-source voltage mismatch, ΔV_{GS} , of the

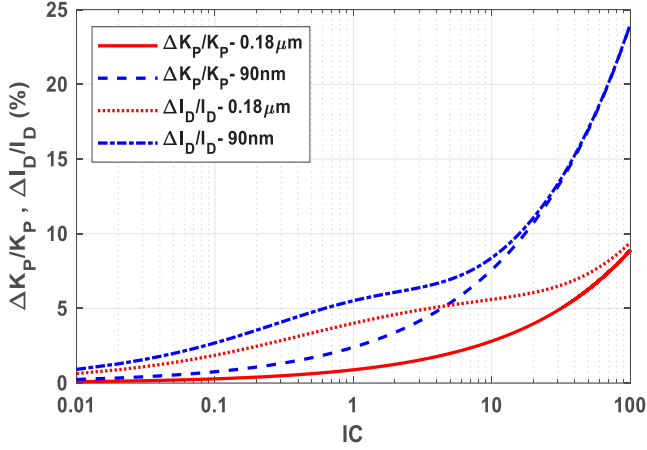


Fig. 13. Relative transconductance mismatch, $\Delta K_p/K_p$, and relative drain current mismatch, $\Delta I_D/I_D$, of an nMOS device versus the inversion coefficient for 90nm and 180nm CMOS processes at a drain current of 100 μA

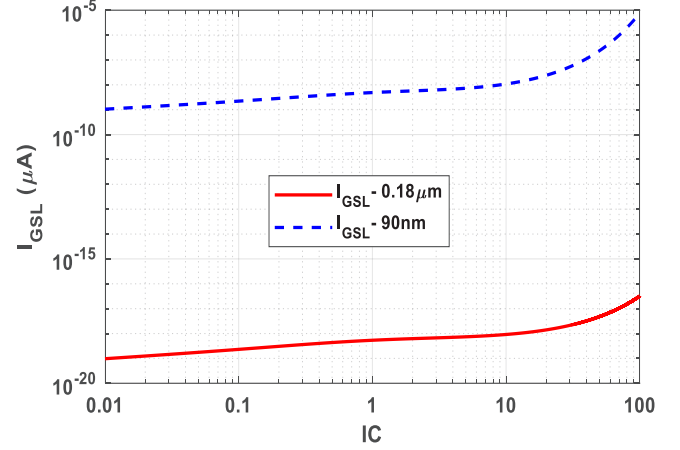


Fig. 14. Gate-source leakage current, $I_{(GS)}$, of an nMOS device versus the inversion coefficient for 90nm and 180nm CMOS processes at a drain current of 100 μA .

nMOS device versus the inversion coefficient in 90nm and 180nm CMOS processes at a drain current of 100 μA . The figure indicates that as technology shrinks, both ΔV_T and ΔV_{GS} increase, with a more significant rise in the SI region due to velocity saturation caused by small geometry effects.

Fig. 13 shows the trends in the relative transconductance mismatch, $\Delta K_p/K_p$, and the relative drain current mismatch, $\Delta I_D/I_D$, of the nMOS device versus the inversion coefficient in 90nm and 180nm CMOS processes at a drain current of 100 μA . The figure reveals that as technology shrinks, both $\Delta K_p/K_p$ and $\Delta I_D/I_D$ increase to moderate values in the WI and MI regions, with a significant rise in the SI region due to velocity saturation effects.

3- 7- Gate-Source Leakage Current

Fig. 14 illustrates the trend of the gate-source leakage current, $I_{(GS)}$, of the nMOS device versus the inversion coefficient in 90nm and 180nm CMOS processes at a drain current of 100 μA . The figure shows that as technology shrinks, $I_{(GS)}$ increases to moderate values in the WI and MI regions, with a significant rise in the SI region due to velocity saturation effects.

3- 8- Figure of merit for low-power RF designs

The product of transconductance efficiency, g_m/I_D , intrinsic bandwidth, f_{Ti} , and intrinsic voltage gain, A_{Vi} , is a figure of merit for MOS devices that can be defined as follows:

$$FOM = (g_m/I_D \cdot f_{Ti} \cdot A_{Vi}) \quad (4)$$

Fig. 15 illustrates the trend of FOM for the nMOS device versus the inversion coefficient in 90nm and 180nm CMOS

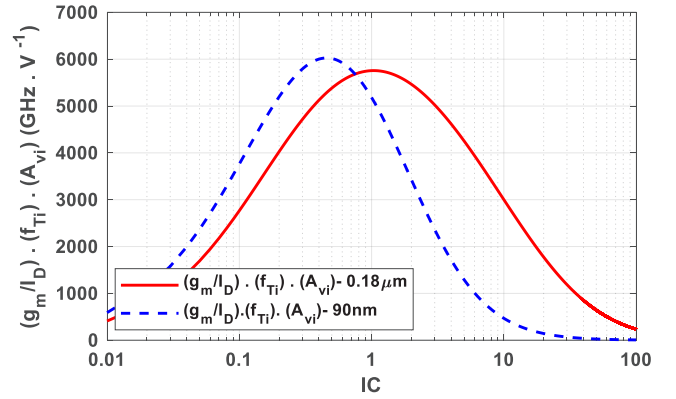


Fig. 15. FOM of an nMOS device versus the inversion coefficient for 90nm and 180nm CMOS processes.

processes at a drain current of 100 μA . The figure indicates that as technology shrinks, FOM increases slightly. Notably, the maximum values for both processes occur in the MI region, highlighting the significance of this region for low-voltage and low-power designs.

4- Integrating Performance Tradeoffs in the MOSFET Operational Plane

Based on the results from Sections 3-1 to 3-7, the MOSFET operating plane illustrated in Fig. 16 depicts performance trade-offs in terms of the inversion coefficient and fabrication process (technology shrinking) at a constant bias current. Each MOSFET or its corresponding group operates at a point on this plane based on its inversion coefficient and fabrication process. Operation in the weak and

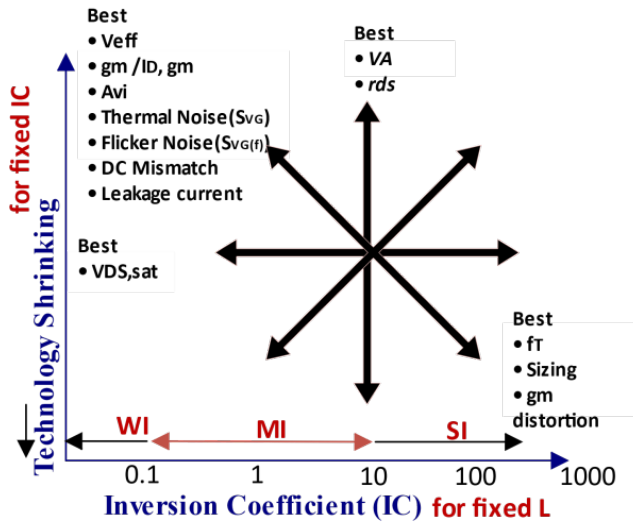


Fig. 16. The MOSFET operating plane illustrating analog performance trade-offs in the MOS device versus the inversion coefficient and fabrication process (technology shrinking) at a constant bias current.

moderate inversion regions (left side of the plane) optimizes transconductance, transconductance efficiency, and intrinsic voltage gain while minimizing gate-referred thermal and flicker noise voltage densities, effective gate-source and drain-source saturation bias voltages, and gate-source leakage current. At low inversion coefficients, the large aspect ratio ($S=W/L$), channel width, gate area, and capacitors reduce intrinsic bandwidth and DC mismatches of gate-source voltage and drain current. In contrast, operation in the strong inversion region with high inversion coefficients (right side of the plane) reduces transconductance, transconductance efficiency, and intrinsic voltage gain while increasing gate-referred thermal and flicker noise voltage densities, effective gate-source and drain-source saturation bias voltages. High inversion coefficients result in smaller aspect ratios, channel widths, gate areas, and capacitors, leading to increased intrinsic bandwidth and DC mismatches of gate-source voltage and drain current. Additionally, operating at high inversion coefficients enhances the device's linearity.

As technology shrinks (moving towards the bottom of the operating plane), the dimensions, drain-source resistance, Early voltage, intrinsic voltage gain, transconductance, and transconductance efficiency of the MOS device decrease. Additionally, intrinsic bandwidth increases, and the device's linear performance improves. However, increased technology shrinking also leads to higher gate-referred thermal and flicker noise voltage densities, as well as greater DC mismatches in gate-source voltage and drain current, effective gate-source and drain-source saturation bias voltages, and gate leakage current.

5- Conclusions

This paper investigates the impact of technology shrinking on MOS device performance, focusing on the key parameter IC in 90nm and 180nm CMOS processes. By plotting MOS device characteristics against IC in these two technologies, the effects of reduced channel length and device geometry from the WI to SI regions are illustrated. For a given drain current in the saturation region, performance trade-offs of the MOS device are summarized on a MOSFET operating plane, helping to identify the optimal design region for active circuit devices with technology shrinking.

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