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# Analysis of a Simplified 13-Level Inverter using Reduced Switched Capacitor Technology

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**Abstract:**

A novel Multi-level Inverter (MLI) with reduced Switched Capacitor (SC) is designed due to its aids of low component count and low-cost implementation. This paper introduces a novel SC-MLI to achieve increased number of output voltage levels with reduced component requirements. Henceforth, 13 level inverter is deployed using 14 switches, 3 capacitors and a single diode, in which voltage through capacitors is continued at required magnitude during the switching operation by utilizing Pulse Width Modulation (PWM) generator. By inducing 13 level reduced SC enables to attain improved voltage boosting with high voltage balancing ability thereby, providing better quality output to load. Thereby, the proposed approach concentrates on designing a reduced SC-MLI for achieving higher output voltage with desired output quality by utilizing very small number components, thereby reducing the size and cost of implementation. Furthermore, system is executed using MATLAB/Simulink and obtained result depicts that proposed system attained enhanced system performance with efficiency (98.50%) with increased amount of output voltage levels.

**Keywords:**

Switched Capacitor, Multi-Level Inverter, PWM generator, Reduced switch 13 level MLI, Power Quality Enhancement.

## 1. Introduction

Due to increased demand of higher electric power conversion in high power application and power industry, leaded to developed of MLI, which plays an important role in enhanced power conversion [1]. MLI's are used in various aspects of power conversion system such as electric power industry, reactive power compensation, Renewable Energy Resources like wind, thermal power plant and Photovoltaic (PV) due to their ability to provide higher power with high voltage transmission and quality output [2]. The major objective for considering MLI's are to attain reduced THD with reduced voltage stress and increased fault-tolerance [3]. Conventional MLI's are divided into three levels namely Neural-Point-Clamped (NPC) MLI, Flying Capacitor (FC) and Cascaded H-Bridge (CHB) however, these inverters struggled with certain drawbacks like voltage imbalance and required increased components for attaining higher output voltage levels [4].

In order to overcome the issues associated with NPC, FC and CHB, Switched Capacitor based MLI are introduced which is capable of maintaining voltage balance along with reduced losses that occurs during switching operations [5]. By inducing SC with MLI achieves the ability to boost input voltage, self-balanced capacitor voltage and minimized usage of DC sources [6]. Furthermore, the implementation of SC-MLI generates large number of output voltage with reduced component counts hence, they are considered as a best option for higher power conversion system [7]. Initially, 5 level MLI's are designed to attain enhanced output voltage waveform with reduced harmonics, Nevertheless, it did not provide desired level of voltage gain [8]. Hence, 7 level MLI's are introduced which nine level SC-MLI is innovated for obtaining double voltage gain with self- balancing of voltage and capacitor by utilizing eleven reduced voltage stress with improved switching operation in spite of that, they still cannot produce desired number of output voltage and struggles with high complexity [10]. Thus, to further improve SC-MLI system, eleven level inverter is developed to enhanced voltage boosting, increased output levels with reduced THD and voltage stress but they required large number of components and DC sources [11]. Henceforth, 13 level

SC-MLI is designed to attain enlarged output voltage levels with reduced component requirement, thereby producing better quality power output.

## 2. Proposed Modelling

A novel 13 level SC-MLI system is designed to produce large number of voltage level with better quality output waveform along with reduced component requirements. The initial working stage of the developed system starts with the input DC supply that is connected to the inverter for generating power quality outputs. In addition to that, PWM generator is connected to produce PWM pulses for attaining low frequency modulation to achieve enhanced switching operation with stable system performance. The block diagram of 13 level SC- MLI is depicted in Fig. 1.

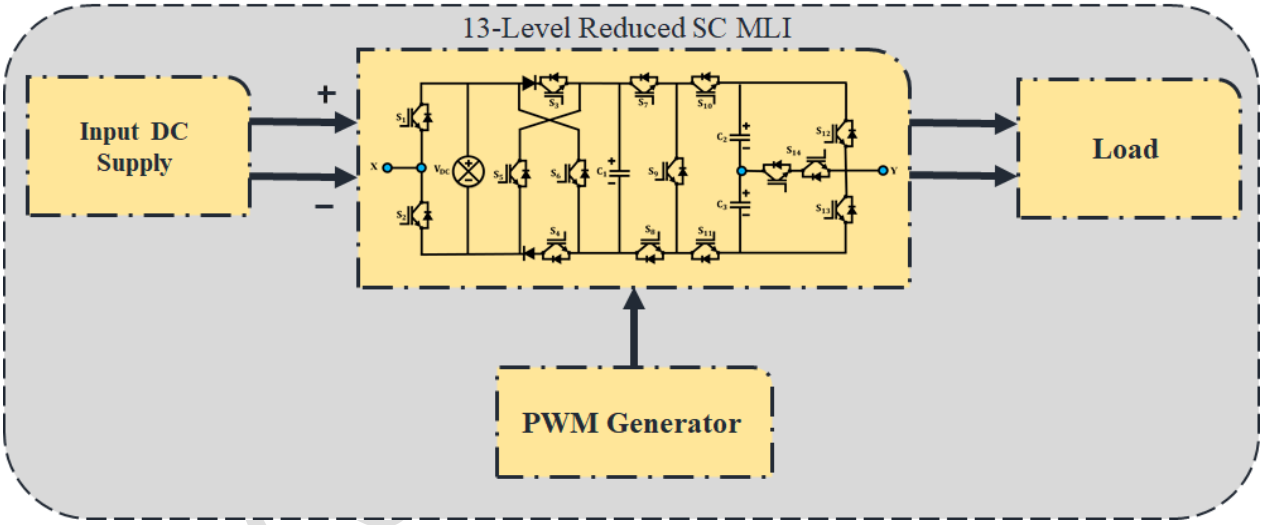



Fig. 1. Novel 13 Level SC-MLI Block Diagram

The fundamental objective for designing the 13 level SC-MLI system is to achieve maximum output voltage levels with minimal requirement of components for attaining stable and reliable energy conversion system making it well suited for higher power applications. Therefore, the developed system assures enhanced efficiency and higher output voltage levels with reduced losses.

## 2-1- Modelling of 13 Level Inverter proposed Modelling

A reduced Switched Capacitor 13 level MLI method is deployed for achieving maximum number of output voltage level with reduced switches and other required components. 13 level –MLI consists of fourteen switches $S_1$ , $S_2$ , $S_3$, $S_{14}$ , 3 capacitors $C_1$ , $C_2$ and $C_3$ and a single DC source, as illustrated in Fig. 2 and Fig. 3 depicts modes of operation.

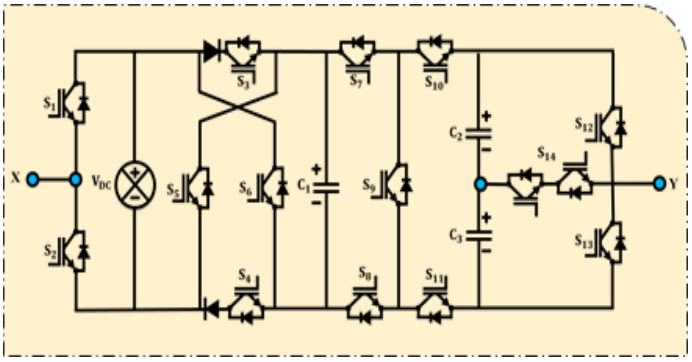
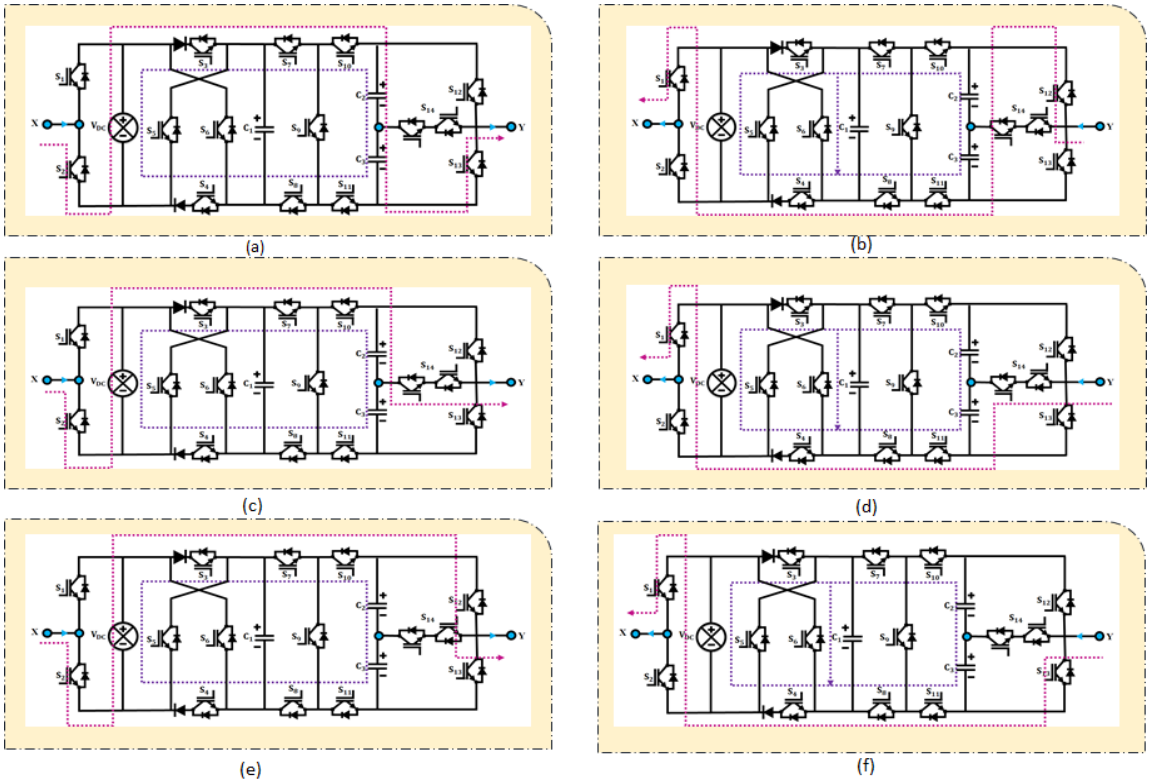



Fig. 2. Circuit design of 13 level SC-MLI



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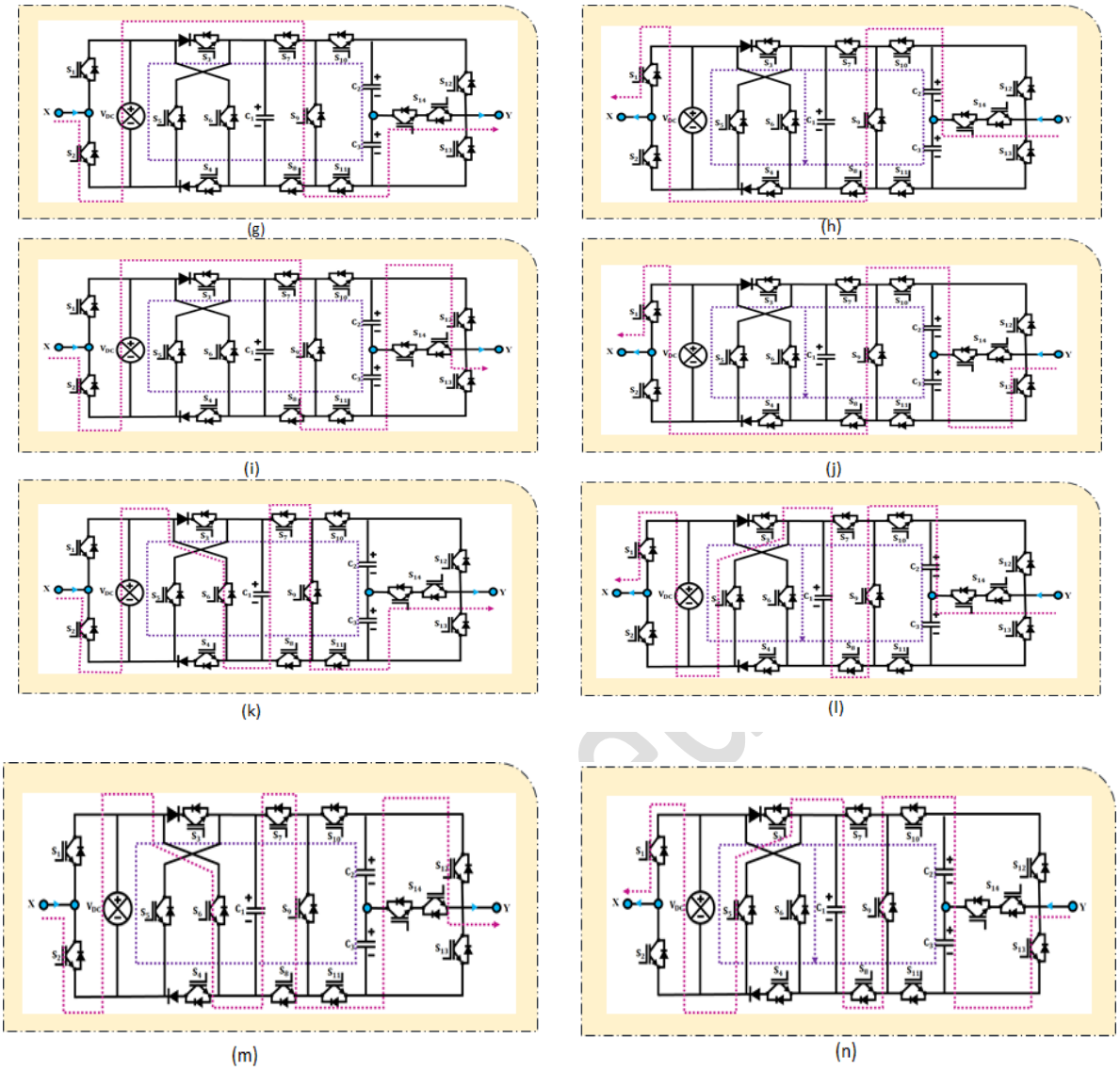


Fig. 3. Modes of Operation

During various switching modes of operation $S_1$ $S_2$ , $S_5$ $S_6$ and $S_{12}$ $S_{13}$ pairs of switches works in complementary mode for attaining improved switching efficiency. Thus, this system generates 13 different levels of output voltages such as 3V, 2.5V, 2V, 1.5V, 1V, 0.5V during positive cycle and -3V, -2.5V, -2V, -1.5V, -1V, -0.5V during negative cycle respectively. Henceforth, the fundamental working process of 13 level SC-MLI consists of 7 modes consecutively which are listed in Table 1 below,

Table 1. Modes of Operation for 13 level SC-MLI

| Modes | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | $S_8$ | $S_9$ | $S_{10}$ | $S_{11}$ | $S_{12}$ | $S_{13}$ | $S_{14}$ | V |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **7** | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 3V |
| **6** | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 2.5V |
| **5** | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 2V |
| **4** | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1.5V |
| **3** | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1V |
| **2** | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0.5V |
| **1** | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0V |
| **1** | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0V |
| **2** | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | -0.5V |
| **3** | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | -1V |
| **4** | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | -1.5V |
| **5** | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | -2V |
| **6** | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | -2.5V |
| **7** | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | -3V |

**Mode 1 :** In this mode, Switches $S_2$ , $S_3$, $S_4$ , $S_7$, $S_8$ , $S_{10}$, $S_{11}$ and $S_{13}$ are kept in ON condition where capacitor $C_1$ is stored and $C_2$ is charged to 0.5 $V_{DC}$ since, all the capacitors are linked parallel to input supply. Similarly, for producing 0V, switches $S_1$, $S_3$, $S_4$, $S_7$, $S_8$, $S_{10}$, $S_{11}$ and $S_{12}$ are turned ON respectively which are shown in Fig. 3 (a) and (b).

**Mode 2:** Switches $S_2$ , $S_3$, $S_4$ , $S_7$, $S_8$ , $S_{10}$, $S_{11}$ and $S_{14}$ are kept in ON condition wherever capacitors $C_1$ , $C_2$ and $C_3$ are linked parallel input source. Thus, $C_1$ is charged to $V_{DC}$ and $C_2$ , $C_3$ are charged to 0.5 $V_{DC}$. Similarly, to attain -0.5 V, switches $S_1$, $S_3$, $S_4$, $S_7$, $S_8$, $S_{10}$, $S_{11}$ and $S_{14}$ are turned ON respectively which are displayed in Fig. 3 (c) and (d).

**Mode 3:** In this mode, Switches $S_2$ , $S_3$ , $S_4$ , $S_7$, $S_8$ , $S_{10}$, $S_{11}$ and $S_{12}$ are kept in ON condition where capacitors $C_1$ , $C_2$ and $C_3$ are linked parallel DC source. Thus, $C_1$ is charged to $V_{DC}$ and $C_2$ , $C_3$ are charged to 0.5 $V_{DC}$. Similarly, to attain -1 V, switches $S_1$, $S_3$ , $S_4$, $S_7$ , $S_8$, $S_{10}$ , $S_{11}$ and $S_{13}$ are turned ON respectively which are displayed in Fig. 3 (e) and (f).

10.22060/EEJ.2025.24349.5690

**Mode 4:** In this mode, Switches $S_2$, $S_3$, $S_4$, $S_7$, $S_9$, $S_{11}$ and $S_{14}$ are kept in ON condition where $C_1$ is charged $V_{DC}$ and $C_3$ discharges kept energy to load. Similarly, to attain -1.5 V, switches $S_1$, $S_3$, $S_4$, $S_8$, $S_9$, $S_{11}$ and $S_{14}$ are turned ON respectively which are shown in Fig. 3 (g) and (h).

**Mode 5:** In this mode, Switches $S_2$, $S_3$, $S_4$, $S_7$, $S_9$, $S_{11}$ and $S_{12}$ are kept in ON state where $C_1$ is connected in series thus, releases the stored energy. Similarly, to attain -2V switches $S_1$, $S_3$, $S_4$, $S_8$, $S_9$, $S_{10}$ and $S_{13}$ are turned ON respectively which are displayed in Fig. 3 (i) and (j).

**Mode 6:** In this mode, Switches $S_2$, $S_6$, $S_7$, $S_9$, $S_{11}$ and $S_{14}$ are kept in ON condition where $C_1$ and $C_3$ are linked in series releases stored energy to load. Similarly, to attain -2.5V, switches $S_1$, $S_5$, $S_7$, $S_9$, $S_{11}$ and $S_{14}$ are turned ON respectively which are displayed in Fig.3 (k) and (l).

**Mode 7:** In this mode, Switches $S_2$, $S_6$, $S_7$, $S_9$, $S_{11}$ and $S_{12}$ are kept in ON condition where $C_1$, $C_2$ and $C_3$ are connected in series releases stored energy to load. Similarly, to attain -3V, switches $S_1$, $S_5$, $S_8$, $S_9$, $S_{11}$ and $S_{13}$ are turned ON respectively which are displayed in Fig. 3 (m) and (n).

In multilevel inverter topologies, simultaneous switch conduction leads to in short-circuit issues. To address this, the proposed 13-level SC-MLI uses complimentary switching control, with each pair of switches operating in opposite modes. The PWM generator synchronises gating pulses with proper dead-time intervals between transitions. This method effectively eliminates shoot-through problems and ensures the safe operation of all semiconductor devices during the switching cycle. Therefore, implementation of 13 level SC MLI produce greater number of voltage output levels with reduced components requirement thus, making it applicable for higher power conversion application.

**2-2- Modelling of Capacitance Selection**

Capacitance Selection is one among the vital part of the SC system as they are responsible for ripple loss, size and cost. Hence, choosing the optimum values of capacitance significantly impact on the SC performance which depend on the following aspects time of discharging, extreme load current and power factor. Therefore, selecting capacitance value is considered crucial and maximum charge released through capacitor is given by,

$$Q_{ci} = \int_{\theta_i}^{\pi-\theta_i} I_m \sin\left(\omega t - \phi\right) dt \tag{1}$$

Where $\theta_i$ represents initial discharging time and $\pi - \theta_i$ represents final discharging period, $\phi$ represents load power factor angle, $I_m$ represents maximum load current. Hence, the value of capacitance must fulfil the below discussed conditions,

$$C_i \geq \frac{\Delta Q_{ci}}{\Delta V_i} \tag{2}$$

Given a load that is entirely resistive, the maximum voltage ripple is as follows:

$$\Delta V_i = \frac{\Delta Q_i}{C_i} \tag{3}$$

$$\Delta V_1 = \frac{1}{\omega\, CR_l} \int_{\theta_3}^{\pi-\theta_i} 2.5V_{DC} dt + \frac{1}{\omega CR_l} \int_{\theta_4}^{\pi-\theta_i} 3V_{DC}\, dt \tag{4}$$

$$\Delta V_1 = \frac{V_{DC}}{\omega CR_l} \left[5.5\pi - 5\,\theta_3 - 6\,\theta_4\right] \tag{5}$$

$$\Delta V_2 = \frac{1}{\omega\, CR_l} \int_{\theta_1}^{\pi-\theta_i} 1.5V_{DC} dt + \frac{1}{\omega CR_l} \int_{\theta_2}^{\pi-\theta_i} 2V_{DC}\, dt + \frac{1}{\omega CR_l} \int_{\theta_3}^{\pi-\theta_i} 2.5V_{DC}\, dt + \frac{1}{\omega CR_l} \int_{\theta_4}^{\pi-\theta_i} 3V_{DC}\, dt \tag{6}$$

$$\Delta V_2 = \frac{V_{DC}}{\omega C R_1}\left[9\pi - 3\theta_1 - 4\theta_2 - 5\theta_3 - 6\theta_4\right] \tag{7}$$

Likewise, $\Delta V_3$ is calculated. Furthermore, the time duration for Discharging of the capacitor is expressed as (8) and (9), where represents fundamental frequency

$$\theta_4 = \frac{\sin^{-1}\left(\frac{2.5}{3}\right)}{2\pi f_0} \tag{8}$$

$$\theta_3 = \frac{\sin^{-1}\left(\frac{2}{3}\right)}{2\pi f_0} \tag{9}$$

Hence, by using the above mentioned calculations enables to attain better capacitance selection which in turn leads to better system performance thereby, providing reduced ripple losses and minimised cost of implementation.

**2-3- Modelling of Power Loss Analysis**

Power loss is measured on the basis of three categories namely switching losses, conduction losses and ripple losses.

***Switching losses***

These losses occur due to transition of switching conditions which is stated as switched-on and switched-off, of switches therefore, power loss is calculated using,

$$P_{on,sw} = \frac{1}{6} f_0 \left(V_{on} I_{on} T_{on}\right) \tag{10}$$

Similarly, power losses during turn-off is measured using,

$$P_{off,sw} = \frac{1}{6} f_0 \left(V_{off} I_{off} T_{off}\right) \tag{11}$$

Where $V_{on}$ , $V_{off}$ is voltage occurring across switches throughout switched-on and switched-off, conditions, $I_{on}$ , $I_{off}$ stands current across switches and $T_{on}$ , $T_{off}$ stands time throughout which switches are turned ON and OFF henceforth, overall switching losses is obtained by,

$$P_{sw} = \sum_{n=1}^{13}\sum_{m=1}^{14}\left(P_{on,sw,m} + P_{of,sw,m}\right) \tag{12}$$

Where $n and k$ denotes number of levels and switches.

***Conduction losses:***

These types of losses occurs owing to power degeneracy in switches and diodes when current passes via them and are measured separately,

$$P_{c,sw} = V_{on,sw}\ I_{sw,avg} + I^2_{sw,rms}\ R_{on,sw} \tag{13}$$

$$P_{c,d} = V_{on,d}\ I_{d,avg} + I^2_{d,rms}\ R_{on,d} \tag{14}$$

Where $V_{on,sw}$ and $V_{on,d}$ denotes voltage switch and diode in ON state, $I_{sw,avg}$ and $I_{d,avg}$ denotes average current of switch and diode. $I^2_{sw,rms}$ and $I^2_{d,rms}$ denotes Root Mean Square (RMS). Consequently, overall conduction losses is expressed using,

$$P_c = \sum_{i=1}^{k}\left(\sum_{j=1}^{n}\left(P_{c,sw} + P_{c,d}\right)\right) \tag{15}$$

Where $n and k$ denotes number of switches and conduction path.

***Ripple losses***

This type of occurs during the charging of capacitor and is measured as following,

$$\Delta V_{Ci} = \frac{1}{Ci}\int_{\theta_i}^{\pi-\theta_i} I_m\left(t\right)\ tdt \tag{16}$$

10.22060/EEJ.2025.24349.5690

Where $\Delta V_{Ci}$, $I_m(t)$ are ripple voltage and ripple current. Thus, ripple losses of capacitor is given as,

$$P_c ap = f / 2 \sum_{(i-1)}^{3} (C_i \Delta V_C i^2) \tag{17}$$

Consequently, overall power loss is considered via adding switching loss, conduction loss and capacitance loss which is expressed as,

$$P_{overall} = P_{sw} + P_c + P_{cap} \tag{18}$$

Finally, efficiency is evaluated by,

$$\% \eta = \left( \frac{P_{out}}{P_{in}} \right) \times 100 \tag{19}$$

$$\% \eta = \left( \frac{P_{out}}{P_{out} + P_{overall}} \right) \times 100 \tag{20}$$

Hence, by utilizing the above mentioned equations, power, conduction and switching losses are evaluated accurately and precisely. Henceforth, ensuring overall enhanced system performance with reduced losses.

## 3. Result and Discussion

The research develops a novel 13 level reduced SC-MLI system for achieving enhanced energy conversion in higher power applications. The deployment of this system ensures to attain maximum output voltage levels with less components and efficacy of established system is calculated by MATLAB/Simulink and comparative study is elaborated below.

Table 2. Specifications of the Proposed 13-Level reduced SC-MLI

| Parameter | Value |
|---|---|
| Switching Frequency $(f_s)$ | $10kHz$ |

| | |
|---|---|
| Load Resistance $(R_L)$ | 25 Ω |
| Load Inductance $(L_L)$ | $20mH$ |
| DC Input Voltage $(V_{dc})$ | $24V$ |
| Capacitor $(C_1, C_2, C_3)$ | $2200\mu F$ |
| Modulation Index $(m_i)$ | 0.9 |
| PWM | Multicarrier PWM |
| Switch | IGBT |

Table 2 lists the specifications for the switches, capacitors, DC source, and load parameters used in 13-level SC-MLI simulation model. These values are chosen based on voltage and current ratings that enable safe operation without exceeding component limits.

### 3-1- Modulation Index 5.9

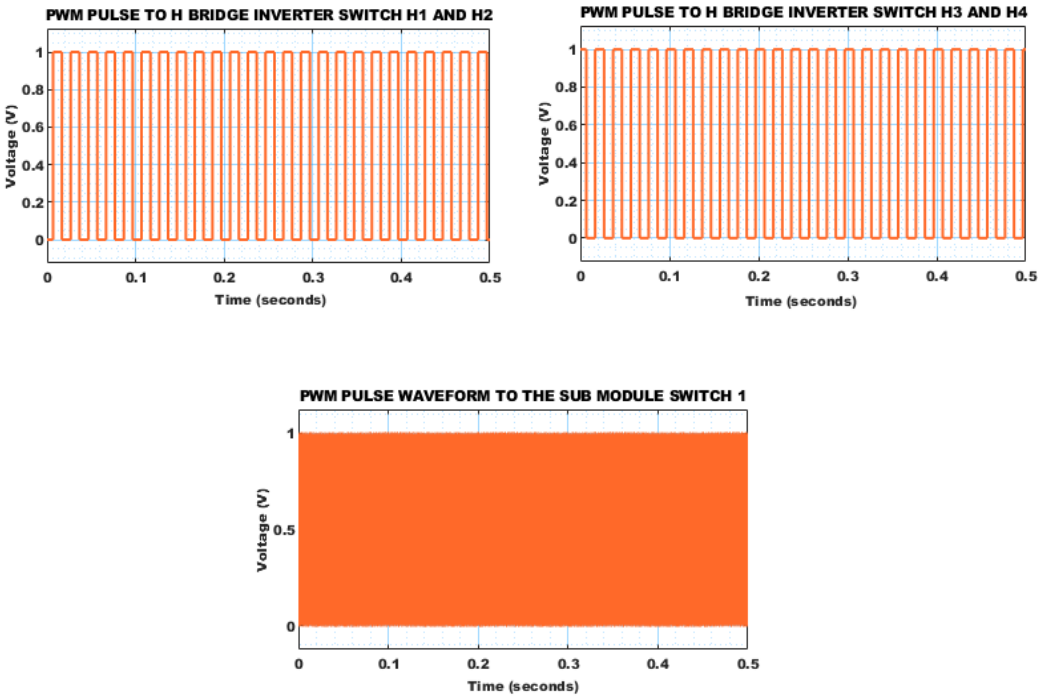


Fig. 4. PWM Pulses waveform

10.22060/EEJ.2025.24349.5690

Fig. 4 represents the PWM pulses waveform for H-Bridge and sub module switch 1 acquired for modulation index 5.9 ,where the first graph shows the PWM pulses for H-Bridge inverter switched $H_1$ and $H_2$, implying high-frequency waveform with voltage ranging between 0 and 1 V over the given time duration. Similarly, second graph also depicts similar patterns as of first.

### 3-2- Zoom View of PWM Pulse Waveform to the Sub Module Switch

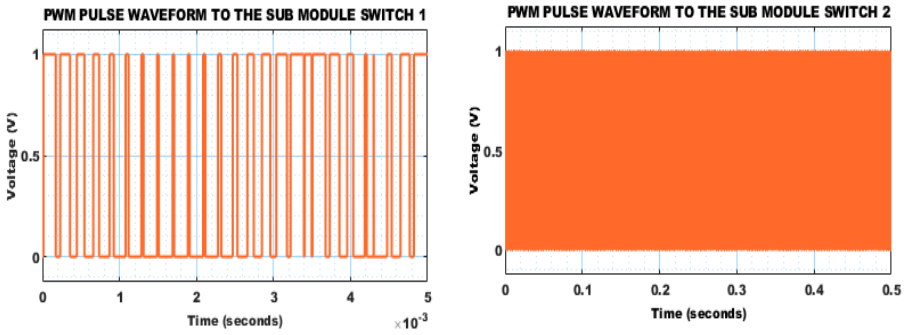


Fig. 5. Sub Module Switch 1 & 2 PWM pulse Waveform

Fig. 5 indicates the PWM pulses for sub module switch 1 & 2, where switch 1 showcases high-frequency voltage waveform ranging between 0 and 1 V throughout time interval $5\times 10^{-3}$ seconds, whereas, PWM pulses for switch 2 showcases higher level of voltage with constant and stable voltage level, indicating enhanced system efficiency.

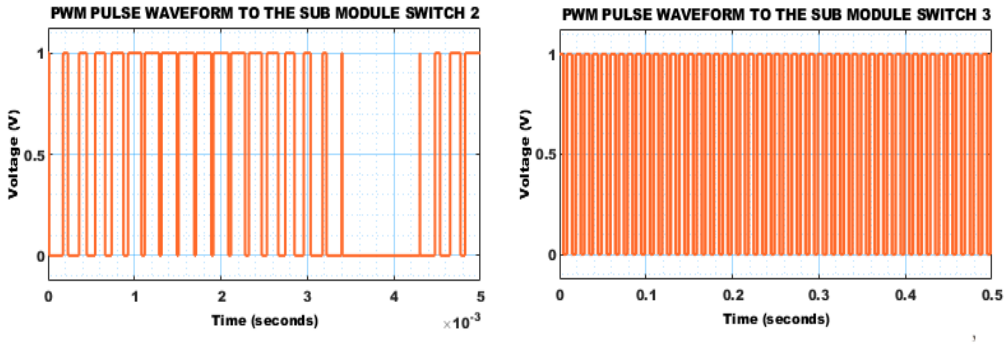


Fig. 6. Sub Module switch 2 & 3 PWM pulse Waveform

Fig. 6 implies the PWM pulses waveform for sub module switch 2 and sub module switch 3, where the PWM pulses waveform for switch 1 depicts inconsistent pattern of voltage high 1V and low respectively. Whereas, PWM pulses for sub module switch 3, depicts consistent and continuous pattern of frequency waveform where voltage is maintained between high 1V and low respectively.

### 3-3- Zoom View of PWM Pulse Waveform to the Sub Module Switch 3

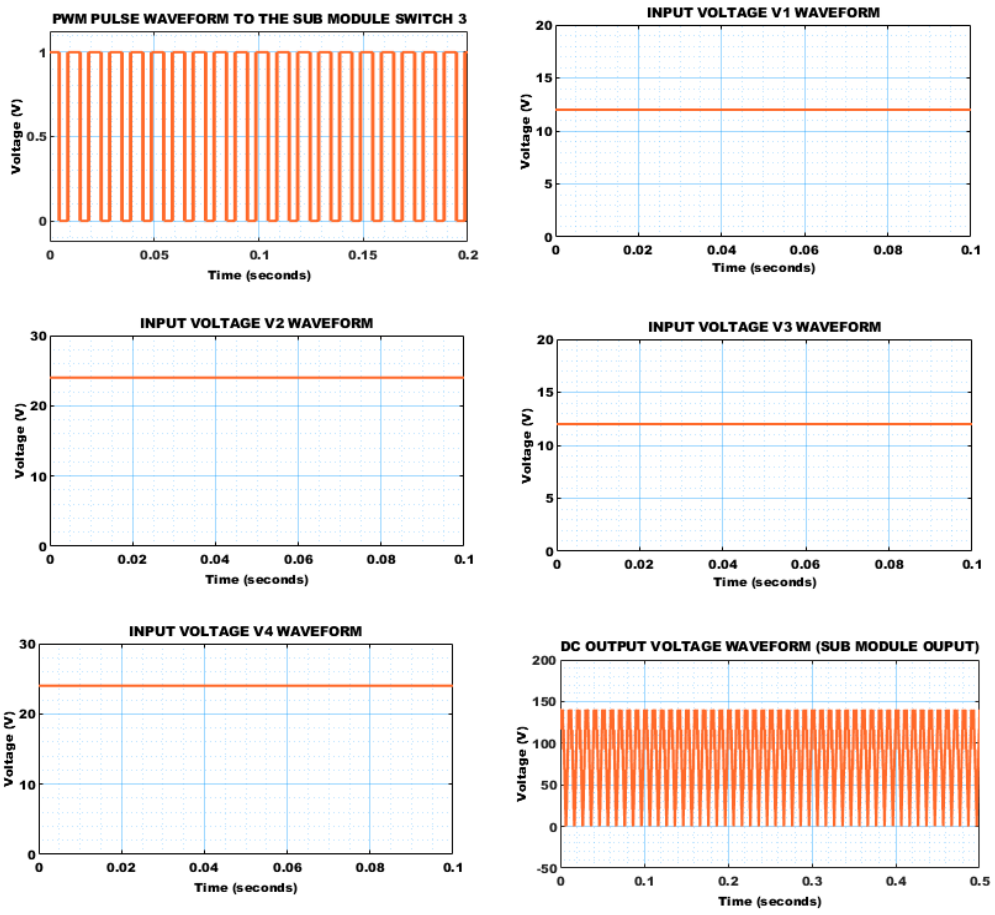


Fig. 7. PWM pulses waveform for sub module switch 3 and Input voltage waveform

Fig. 7 indicates PWM pulses waveform and input voltage waveform, where the first graph show the PWM pulses for sub module switch 3 in which voltage is exhibited inn high frequency rectangular waveform respectively. The second, third, fourth and fifth graph represents the input voltage $V_1$, S , $V_3$ and $V_4$

waveform, where all the four graph depicts consistent and stable voltage of 25V in smooth line, indicating non-fluctuated.

### 3-4- Zoom View of DC Output Voltage Waveform

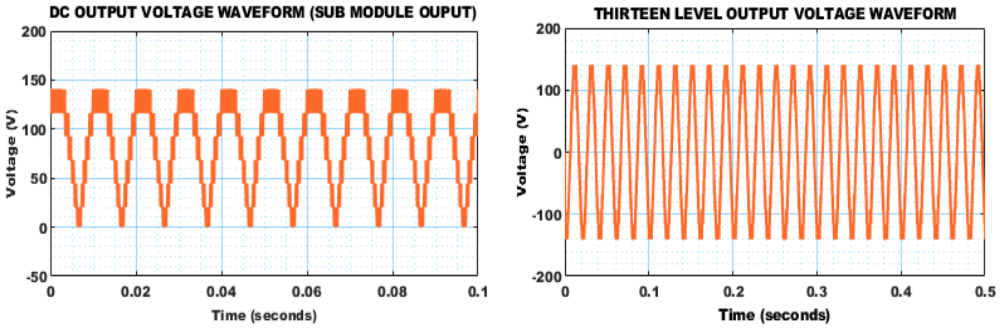


Fig. 8. DC and 13 Level Output Voltage Waveform

Fig. 8 refers to DC output voltage and 13 level output voltage, where the DC output voltage remains consistent within positive half cycle of voltage ranging between 150 V, whereas, 13 level output voltage ranges beyond ± 100 V respectively.

### 3-5- Zoom View of Thirteen Level Output Voltage Waveform

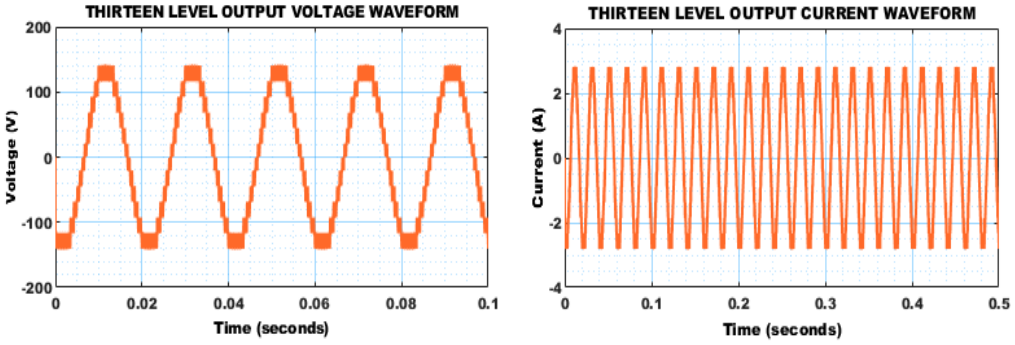


Fig. 9. 13 Level Output voltage and current waveform

Fig. 9 indicates output voltage and current of 13 level inverter where, voltage shows continuous and stable voltage pattern ranging above ± 100 V respectively. While, the 13 level inverter current output depicts that, current remains stable.

### 3-6- Current Waveform

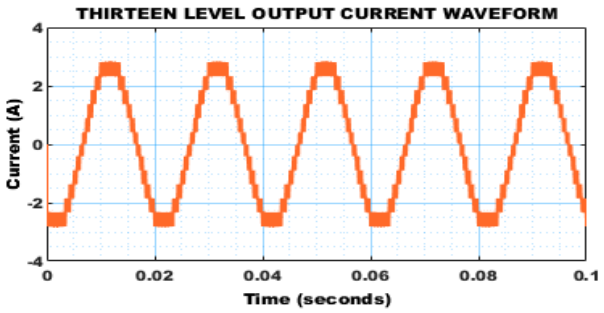


Fig. 10. Output current waveform

Fig. 10 denotes 13 level inverter current output waveform, in which the current exhibits uniform pattern waves with current raging beyond $\pm 2$ A respectively, implying improved system functioning.

### 3-7- Modulation Index 5.3

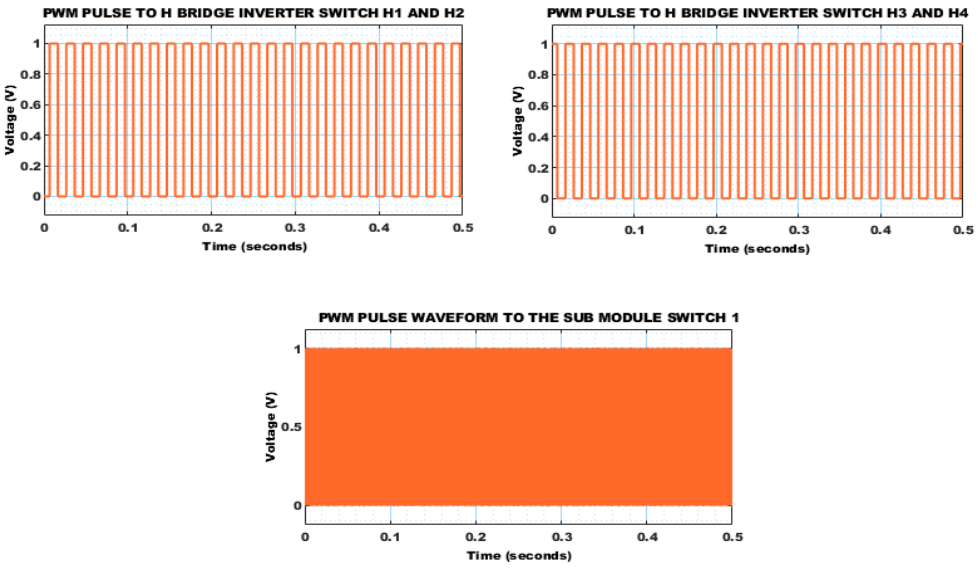


Fig. 11. PWM pulses for H bridge inverter and sub module switch 1

10.22060/EEJ.2025.24349.5690

Fig. 11 represents the PWM pulses for H-Bridge inverter switches and sub module switches. The first and second graph exhibit similar pattern for both the switches $H_1$, $H_2$ and $H_3$, $H_4$ where, for both graph the voltage showcases frequent and continuous rectangular waveform raging between 1 V high and 0 V low respectively. The third graph indicates that the voltage exhibited by sub module switch 1 is high frequency voltage raging between 0 and 1 V through given time duration of 0.5 seconds.

### 3-8- Zoom View of PWM Pulse Waveform to the Sub Module Switch 1

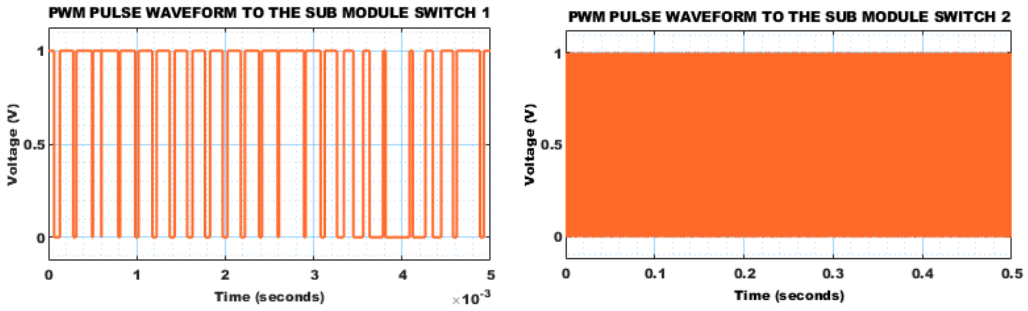


Fig. 12. PWM waveform for sub module switch 1 & 2

Fig. 12 demonstrates the PWM pulse waveform for sub module switch 1 and 2, among which both the switches depicts different wave patterns. Sub module switch 1 shows a slightly non-uniform wave patterns, While, sub module switch 2 depicts consistent and stable wave patterns of high voltage frequencies raging between high 1 V and low 0 respectively.

### 3-9- Zoom View of PWM Pulse Waveform to the Sub Module Switch 2

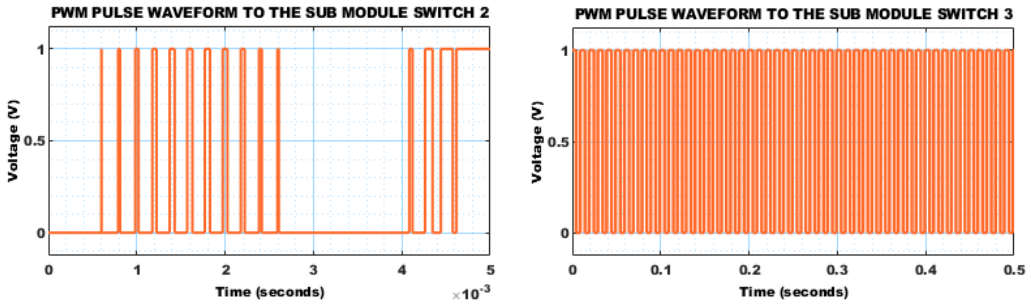


Fig. 13. Sub module switch 2 & 3, PWM pulses waveform

Fig. 13 refers to the PWM pulses waveform for sub module switch 2 and 3, in which switch 1 exhibits moderately non-uniform wave pattern, while switch 3 exhibits frequent and consistent uniform wave patterns of voltage maintained between 1 V respectively.

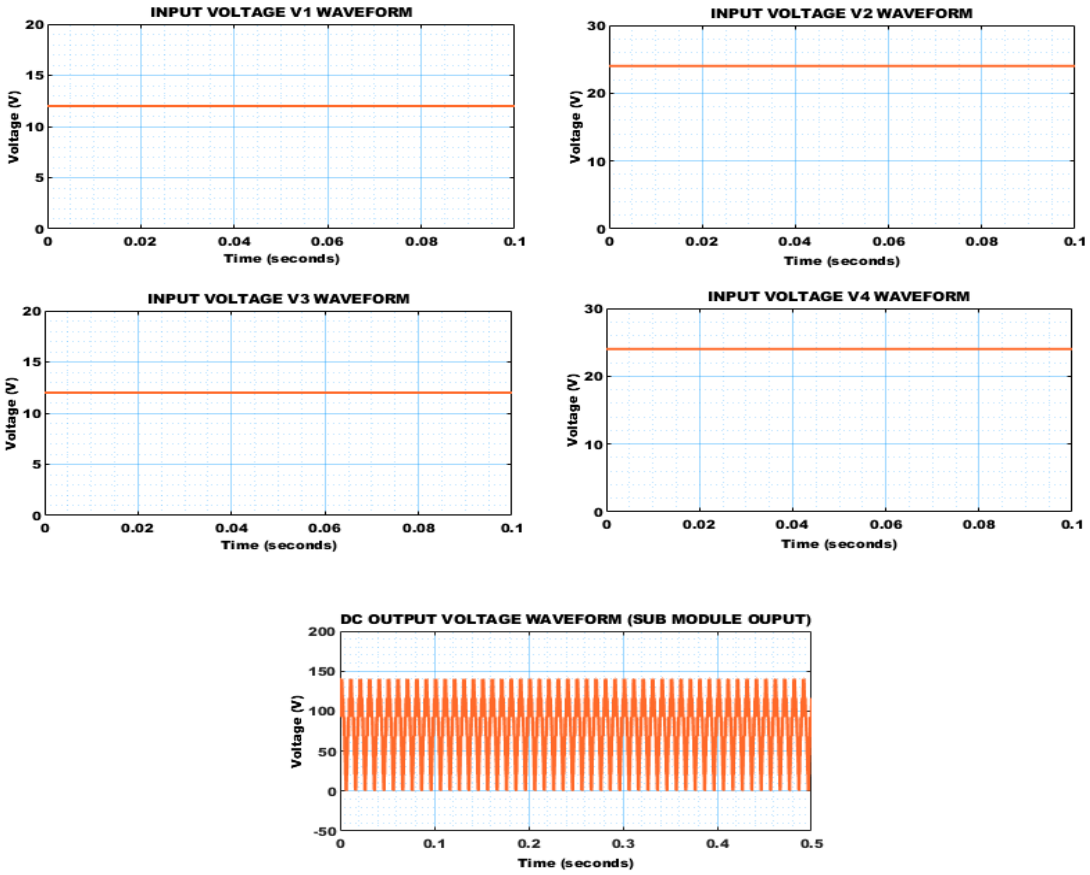


Fig. 14. Input Voltage and DC Output Voltage Waveforms

Fig. 14 represents input voltage waveform and DC output waveform, where all the four input voltage depicts constant and consistent voltage of smooth line which is continuously maintained at particular voltage, the first graph voltage is continued at 13 V, $V_2$ is upheld at 25V, $V_3$ is sustained at 13V and $V_4$ is maintained at 25V respectively, referring to smooth input voltage without any deviations. The last graph depicts the DC output voltage which ranges beyond ± 100 V respectively.

10.22060/EEJ.2025.24349.5690

### 3-10- Zoom View of DC Output Voltage Waveform

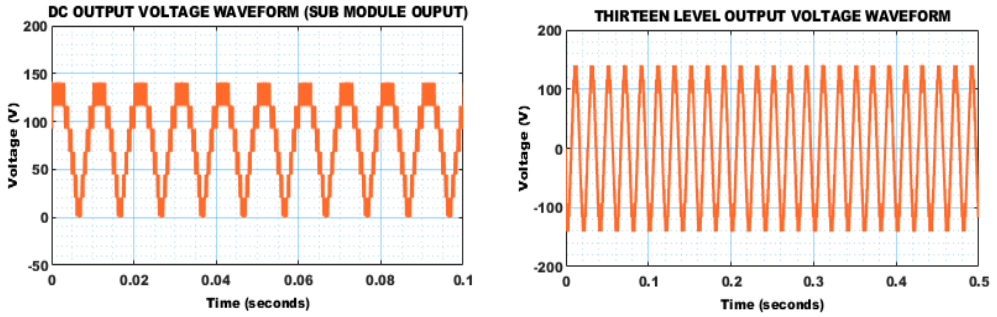


Fig. 15. Output voltage of DC and 13 Level

Fig. 15 showcases the zoom view of output voltage for DC and 13 level waveform, in which the DC output voltage fluctuates between 0 and slightly above 100 V respectively. While, 13 level output voltage waveform exhibits frequent and consistent wave patterns of voltage ranging above ± 100 V respectively.

3.10. Zoom View of Thirteen Output Voltage Waveform

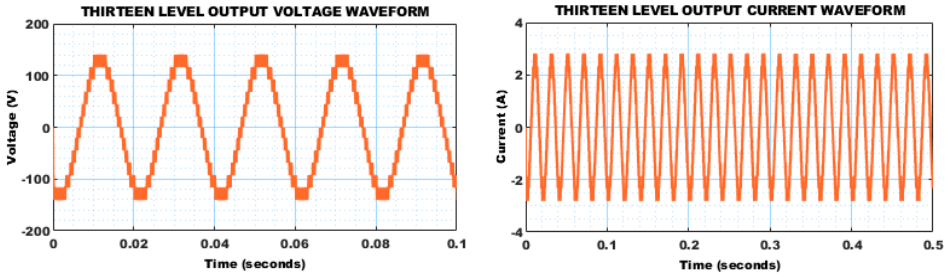


Fig. 16. Output voltage and current waveform for 13 level

Fig. 16 displays output voltage and current of 13 level inverter, where both the voltage and current depicts constant patterns of high frequency waves in which voltage is preserved between ± 100 V and current is maintained ±2 A respectively.

### 3-11- Zoom View of Thirteen Output Current Waveform

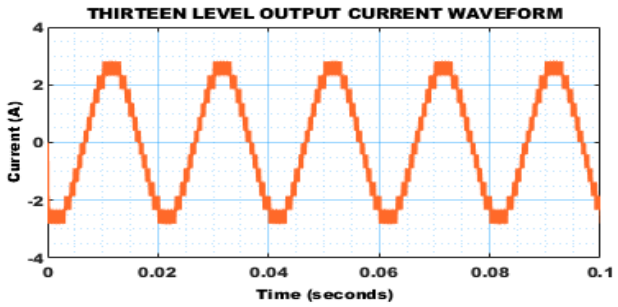


Fig. 17. Output current waveform for 13 level

Fig. 17 indicates the output current exhibited by the 13 level inverter, in which current is attained between ±2 A throughout the depicted time interval of 0.1 seconds respective.

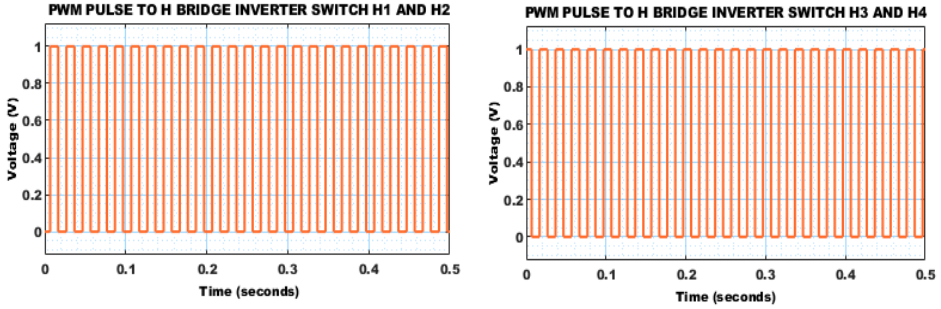


Fig. 18. H-bridge inverter PWM pulses waveform

Fig. 18 implies the H-Bridge inverter PWM pulses for switch $H_1$, $H_2$ and $H_3$, $H_4$. From the above displayed graph it is notable that, both the set of switches show similar frequent rectangular pattern waves of voltage maintained between high 1V and low 0V respectively.

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**3-12- Zoom View of PWM Pulse Waveform to the Sub Module Switch 1**

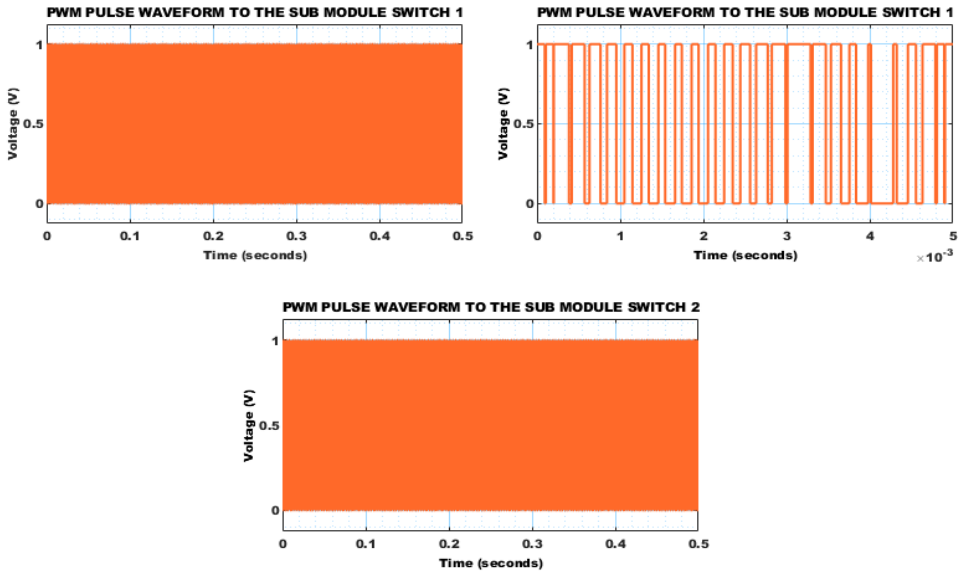


Fig. 19. PWM pulses waveform for sub module switches

Fig. 19 denotes PWM pulses for sub module switch 1 and 2, where first and third graph showcases similar high frequency waves of continuous pattern in which voltage is maintained between high 1 V and low 0 V respectively. In contrast, the second graph exhibits non-uniform patterns of rectangular wave patterns of voltage level ranging between high 1V and low 0 V respectively3.13. Zoom View of PWM Pulse Waveform to the Sub Module Switch 2

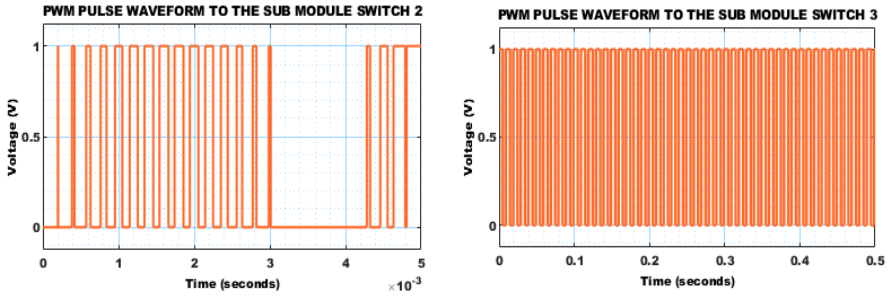


Fig. 20. Switch 2 & 3 PWM pulses waveform

Fig. 20 denotes PWM pulses for sub module switch 2 and 3, in which switch 2 showcases discontinuous rectangular wave patterns throughout the given time duration of $5\times 10^{-3}$ seconds. Whereas, the wave pattern exhibited by sub module switch 3 is frequent and continuous rectangular waves which is maintained at constant voltage levels.

### 3-13- Zoom View of Dc Output Voltage Waveform

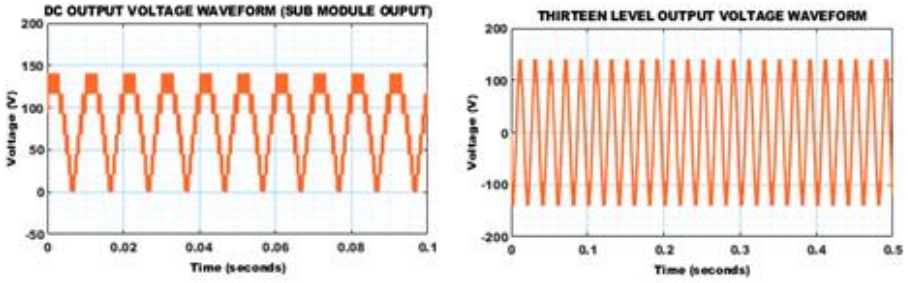


Fig. 21. Waveforms of Output Voltage

Fig. 21 indicates the DC output and 13 level output waveforms, the first graph showcases the DC output voltage of continuous wave pattern in which the voltage is maintained at consistent level from 0 and slightly above 100 V respectively. Whereas, the second graph depicts the 13 level output voltage waveform with consistent frequency wave pattern which are maintained between ± 100 V respectively.

10.22060/EEJ.2025.24349.5690

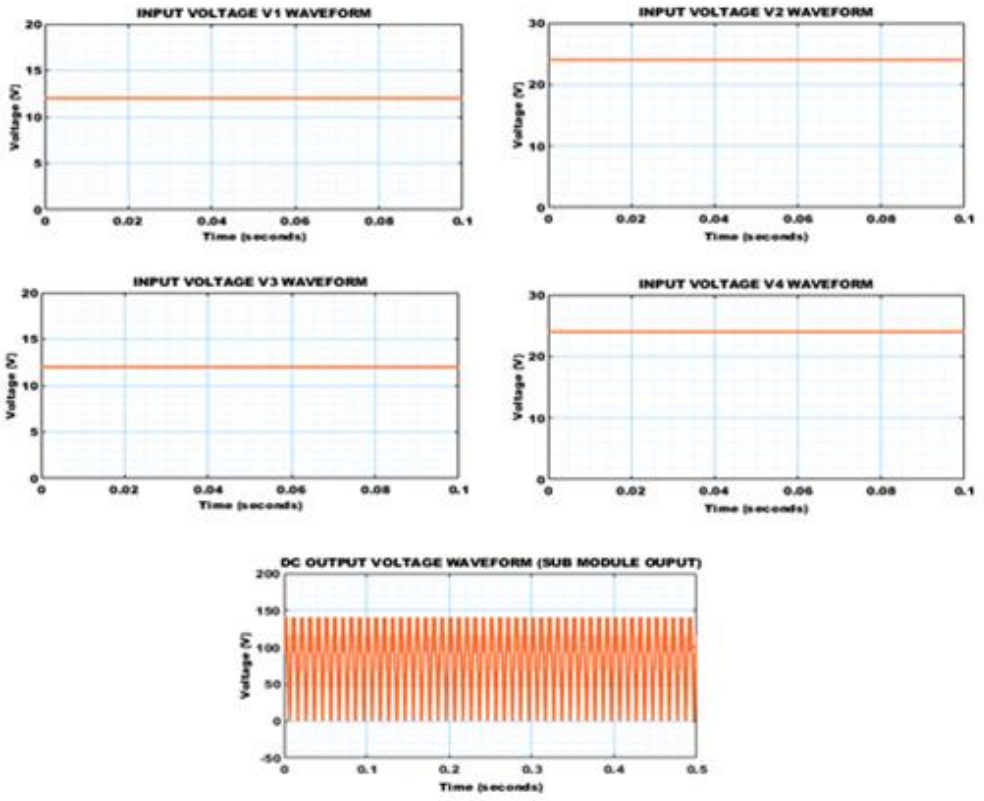


Fig. 22. Input voltage and DC output voltage waveform

Fig. 22 denotes input voltage $V_1$ , $V_2$, $V_3$ and $V_4$ with DC output voltage waveforms. Where $V_1$ and $V_3$ exhibits quite similar voltage of 13V and the smooth line indicates continuous and non-fluctuated voltage input, Similarly, $V_2$ and $V_4$ exhibit same voltage level of 25 V, indicating smooth DC output voltage respectively.

### 3-14- Zoom View of Thirteen Level DC Output Voltage Waveform

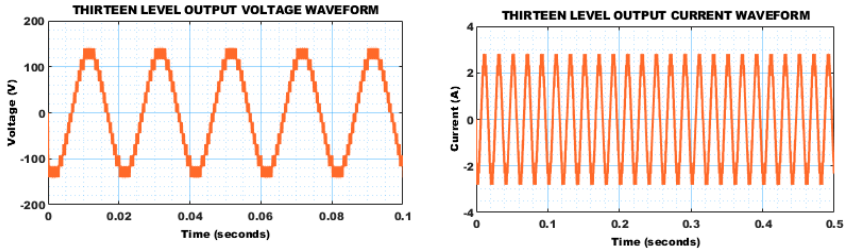

Fig. 23. Waveform for 13 level MLI output voltage and current

Fig. 23 implies zoom view of output voltage and current depicted by 13 level inverter, where the voltage is maintained between ± 100 V and current is maintained between ± 2 A respectively

### 3-15- Zoom View Thirteen Level Output Current Waveform

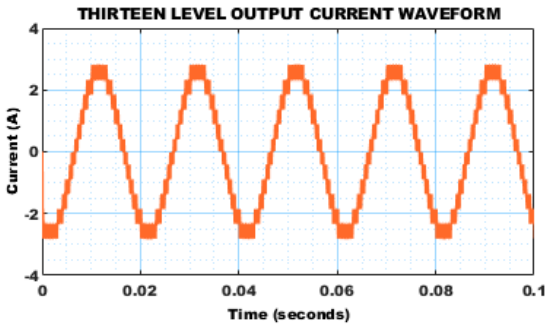


Fig. 24. Output current of 13 level

Fig. 24 demonstrates output current waveform of 13 level inverter, which exhibits the continuous frequency wave patterns of current ranging between ± 2 A respectively, indicating improved and enhanced system functioning.

### 3-16- Zoom View of Thirteen-Level Output Voltage and Current Waveforms of $R_L$ Load

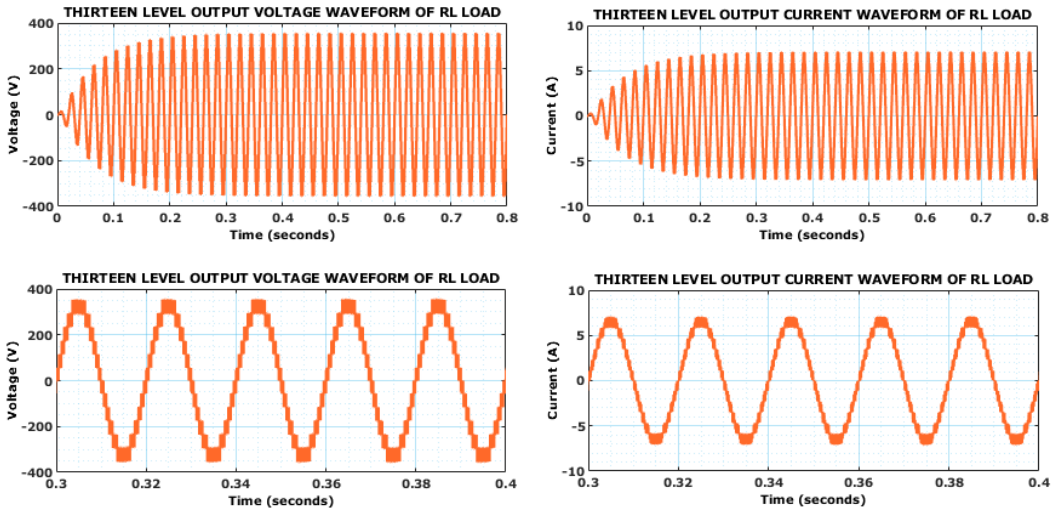

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Fig. 25. 13 Level output voltage and current of $R_L$ load

Fig. 25 show the output voltage and current waveforms of 13-level SC-MLI under $R_L$ load conditions. Output voltage waveform stepped sinusoidal pattern with thirteen unique voltage levels that range from +380 V to -380 V, indicating that many voltage steps generated with minimum distortion. The load current waveform in sinusoidal, with a peak amplitude of ±8.5 A. This indicates proper phase alignment and smooth current response via the inductive-resistive load.

Table 3. Evaluation of proposed MLI with conventional MLI

| Reference | Level | Switches | Capacitors | Dc Sources |
|---|---|---|---|---|
| **[12]** | 7 | 7 | 2 | 1 |
| **[13]** | 9 | 10 | 3 | 1 |
| **[14]** | 9 | 10 | 2 | 1 |
| **[15]** | 13 | 11 | 11 | 1 |
| **[16]** | 13 | 17 | 3 | 1 |
| Proposed | 13 | 14 | 3 | 1 |

Evaluation of suggested 13-level SC-MLI with assorted inverter design currently in use is displayed in Table 3. Compared to other comparable designs, the proposed system uses fewer components of 14 switches, 3 capacitors, and one DC source, to produce 13 output levels. This component reduction raises the inverter's overall efficiency while lowering circuit complexity, cost, and power losses.

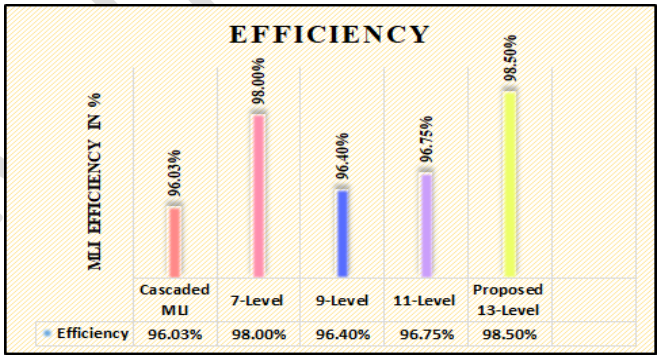


Fig. 26. Efficiency Comparison

Fig. 26 indicates efficiency comparison to determine the performance efficacy of proposed inverter with conventional inverters such as cascaded MLI [17], 7 level [12], 9 level [18] and 11-level [19]. From the

above displayed chart, , the proposed 13 level SC MLI attained higher efficiency of 98.50% while the other MLI's depicted slightly reduced efficacy, thereby, referring to the enhanced overall functioning of the proposed system.

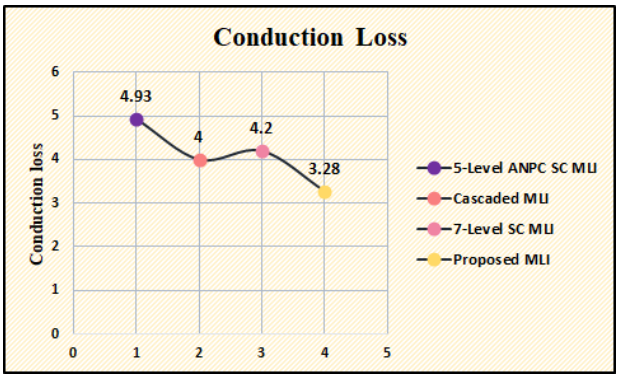


Fig. 27. Conduction Loss

Fig. 27 represents Conduction Loss exhibited by proposed MLI with other traditional MLI's including 5 Level ANPC SC-MLI [20] to determine the performance efficacy of the proposed system. Traditional MLI's showcases quite higher conduction loss when compared to the proposed 13 level MLI, ensuring improved inverter performance with reduced losses.

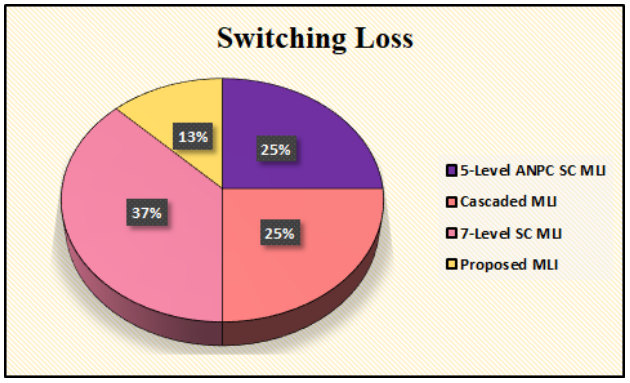


Fig. 28. Switching loss

Fig. 28 showcases the comparison of switching loss exhibited by proposed inverter and other existing inverters. From the above illustrated Pie chart, it is notable that, proposed inverter attained reduced

switching loss of 13 %, whereas, the other inverter attained slightly higher switching losses of 25%, 25% and 37 % respectively.

## 4. Conclusion

This paper exhibits novel 13 Level SC-MLI for achieving high efficiency, with reduced switching and conduction losses. Main objective of this system to attain maximum output voltage with very limited number of components thereby, reducing size and cost of overall system implementation. Henceforth, to analyse performance of proposed system, MATLAB is utilized from obtained results, comparative analysis is performed and from which it is apparent that 13 level SC-MLI attained higher efficiency of 98.50%, maximum voltage levels with reduced component usage, conduction and switching losses. Thus, leading to improved power conversion making is applicable for higher power applications.

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