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Increasing Voltage Gain by New Structure of Inductive Switching DC-DC Converter

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ABSTRACT: In a photovoltaic system, sun light energy is converted to electricity. The generated electricity has a low DC voltage. In order to increase voltage generated by photovoltaic cells (PV), an additive DC-DC converter is required to raise the low voltage to a good level which provides the conditions for connection to DC-DC converters. Low wastes, low costs, and high efficiency are some other specifications of such converters. This paper presents a new structure for an additive DC-DC converter with inductive and capacitor switching for increasing high voltage gain to be used in PV system. It is based on the inductive and non-insulated switching which increases voltage in a duty cycle up to 10 times of input voltage. In addition, using a switch, low elements, and also low voltage stress on the switch is the advantage of this new setup. The easy increasing of levels to reach the higher voltages is another benefit of this structure. The paper continues with the analysis of circuit function and PWM (Pulse Width Modulation) adjustments. PSCAD/EMTDC software is used for confirming the authenticity of the performance of the suggested model. The results are presented.

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1- Introduction

The use of equipment with low cost and high efficiency has always been considered in the industry. Therefore, there are much more demands for increasing the voltage gain of DC-DA converters. Some important applications of such converters are PV systems and ballast lamps with a high charge [1, 2]. Scientifically, additive converter can singly present any voltage gain in the output because its voltage gain relation is $\frac{1}{1-d}$ where d is the duty cycle. As d increases, the gain increases. However, the diode wastes and also voltage stress on the switch increase in practice which finally leads to a reduction of the gain.

Therefore, many efforts have been made and different methods have been presented over the two recent decades to increase voltage gain and the return of such converters [3]. These methods are divided into two groups. One method makes use of the basic structure of additional converter in which capacitors are the intermediate of source and charge [4-6], and as the number of capacitors increases, the number of output voltage classes increases. Capacitor switching were used in some articles. They are called non-insulated converters [7,8]. In the paper [9], more capacitors and diodes have been used to have a higher gain but voltage stress on the switch increased, and the converter return reduced.

Another method is to use inductor and transformer in converters which are called isolated converters, and their mechanism is to transfer energy based on the magnetic concepts. Article [10] presents an additive converter based on inductor in which the inductor's leakage increases as rises.

Some papers have suggested a combination of two methods which have achieved much success [10]; However, the production cost is high.

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This paper presents a new structure of additive DC-DC converter, with inductive and capacitor switching for the photovoltaic system (PV), which can provide any voltage requested in the output by increasing and reducing the classes in addition to high gain voltage and low production costs. The main advantage of this structure is to use a switch and fewer elements than other structures, like the structure proposed in the paper [12]. The existence of serial inductors with capacitors and diodes will limit the current and avoids impact current passing through the circuit.

The paper is organized as it follows. Section 2 explains the converter structure. Section 3describes the converter function in different modes, and Section 4 presents the results of the simulation with PSCAD software.

2- Structure of the suggested converter

Basic Converter:

Figure 1 shows the basic structure of the proposed converter. Three diodes and two inductors are used in this structure. Diodes D_1 and D_2 are turned on and diode D_{12} is turned off in time interval T_{on} ; therefore, inductors L_1 and L_2 are placed parallel to each other and charged by a voltage source, and $v_{L1}=v_{L2}$. Diodes D_1 and D_2 are turned off and diode D_{12} is turned on in time interval T_{off}. The created path puts the inductors L_1 and L_2 in series with the user, and the energy saved in inductors is discharged in the output load $i_{L1}=i_{L2}$.

Proposed Structure

The suggested structure is indicated in Figure 3. The converter consists of n+1 inductors, 3 capacitors, and 3n-1 diodes, where $n \geq 2$. The method used for increasing the classes by increasing a definite number of diodes and inductors in inductor block is shown. Capacitor C_{o2} will cause the correct function of turning on and off the diodes D_{o1} and D_{o2}. In this structure, the function of the converter switching in time intervals T_{on} and T_{off} is the increasing of output voltage by switch S. Ccapacitor C_{o2} and inductors provides inductive and capacitor switching.

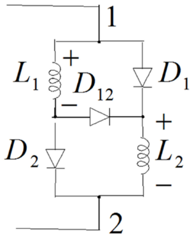
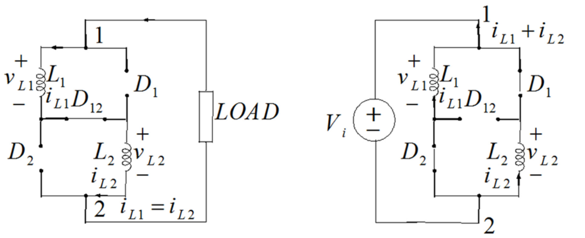


Fig. 1. Inductor Block



(a) **(b)**

Fig. 2. Equivalent Circuit Inductor Block in Time Interval T_{on},T_{off}

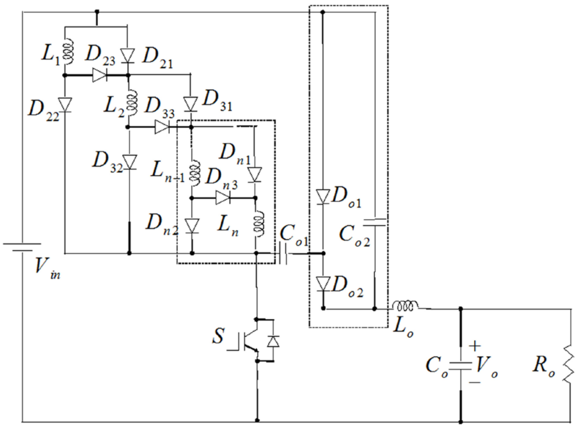


Fig. 3. Structure of Suggested Converter

For asimple analysis, the following hypotheses are considered:

1. power supply voltage is flat without ripple;
2. all elements are deemed ideal;
3. all inductors have the same .amount

3- The function of suggested converter:

Function of Continuous Conduction Mode(CCM)

Circuit analysis in this mode in a time interval T_s after the transient state is as follows:

In time interval $0 \leq t \leq DT_s$: according to Figure 4, switch S is connected in this time interval and diodes D_{21},D_{31},D_{41},...,D_{n1} and D_{22},D_{32},D_{42},...,D_{n2} are in parallel with voltage sources in direct bias. Diodes D_{23},D_{33},D_{43},...,D_{n3} are in adverse bias and off. The voltage of their both sides is equal to v_{in}. Thus, inductors L_1,L_2,L_3,...,L_n are placed in charge path and series to a voltage source. The voltage of their both sides is v_{in}, and also their current reaches i_{Lmax}.

The function of capacitors C_{o1} and C_{o2} with diodes D_{o1} and D_{o2} is analyzed in a way that capacitors C_{o1} is discharged from the previous cycle and its voltage is less than v_{in}. Therefore, diode D_{o1} is in direct bias and is on. Diode D_{o2} is in reverse bias with a voltage equal to v_{Co2} and is off. Consider that capacitor C_{o2} is charged from the previous step and keeps its charge. Capacitor C_{o1} is charged for v_{in} through the path made by the diodes.

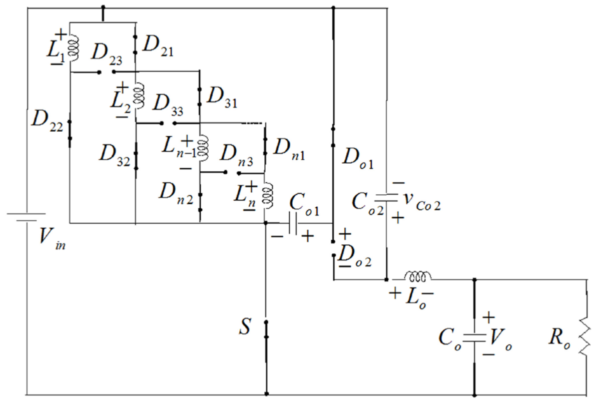


Fig. 4. Circuit in Time Interval T_{on}

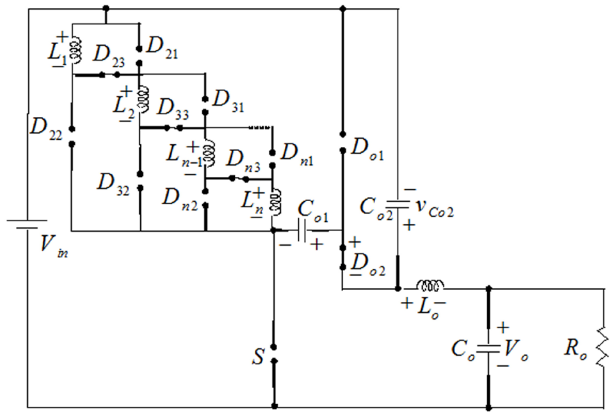


Fig. 5. Circuit in Time Interval T_{off}

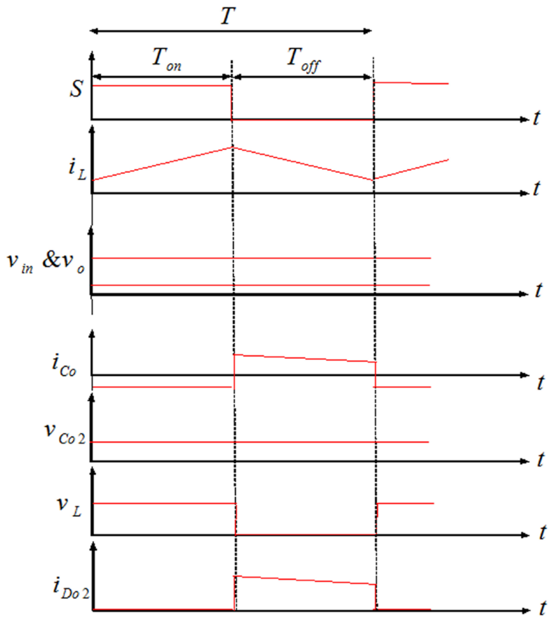


Fig. 6. Form of Waves of Circuit Elements in Mode CCM

According to the given explanations, the following relations are obtained for the time interval T_{on}:
The voltages of inductors are obtained as follows:

$$v_{L_1} = v_{L_2} = \ldots = v_{L_n} = v_{in} \tag{1}$$

Capacitor C_{o1} is fully charged:

$$v_{C_{o1}} = v_{in} \tag{2}$$

The following relation is obtained by KVL in the output circuit loop:

$$v_{Lo} = v_{Co_2} + v_{in} - v_o \tag{3}$$

The voltage of off-diodes included in adverse bias is as follows:

$$v_{D_{23}} = v_{D_{33}} = \ldots = v_{D_{n3}} = -v_{in} \tag{4}$$

$$v_{D_{o2}} = -v_{Co2} \tag{5}$$

The inductors current is obtained by inductor and integration relation:

$$v_L = L\frac{di_L}{dt} \tag{6}$$

$$i_L = \frac{1}{L} v_{in} t + i_{L\min} \tag{7}$$

In time interval $DT_s \le t \le T_s$: switch S is off. Figure 5 indicates the structure in this time interval. Immediately after disconnecting inductors' switch, negative polarity is selected in order to avoid the current disconnection from the previous step; thus, all diodes $D_{21}, D_{31}, D_{41}, \ldots, D_{n1}$ and $D_{22}, D_{32}, D_{42}, \ldots, D_{n2}$ are off. It causes diodes $D_{23}, D_{33}, D_{43}, \ldots, D_{n3}$ to become turned on and diode D_{o2} turns on because a voltage equal to $(n+1)v_{in}$ has been made on its anode. Moreover, reverse bias diode D_{o1} with a voltage equal to the voltage of capacitor C_{o2} turns off. Therefore, the path of the sources of voltage, inductors, and the capacitor C_{o1}, to make series with output load is provided to present the maximum voltage in the output.
Figure 6 indicates the waves of some circuit elements in mode CCM.
The following relations are obtained for the converter function in the second time interval. The inductor's voltage is obtained from KVL by

$$v_{Ln} = \frac{v_{C_{o1}} - v_{C_{o2}}}{n} \tag{8}$$

Since the output voltage is constant, the current of output capacitor C_o is zero; thus, only fixed current $\frac{v_o}{R}$ passes through inductor L_o which makes its voltage zero. In this case, there

$$v_{C_{o2}} = v_o - v_{in} \tag{9}$$

$$v_{Ln} = \frac{2v_{in} - v_o}{n} \tag{10}$$

are the following conditions:
And the following relation is obtained from relation (8):
A bias voltage of off diodes is the second time interval as

$$v_{D_{21}} = v_{D_{31}} = \ldots = v_{D_{n1}} = -v_L \tag{11}$$

$$v_{D_{22}} = v_{D_{32}} = \ldots = v_{D_{n2}} = -v_L \tag{12}$$

$$v_{D_{o2}} = -v_{Co2} \tag{13}$$

follows where the voltage of inductors are deemed the same

$$\frac{1}{T_s}\left(\int_0^{dT_s} v_{in} dt + \int_{dT_s}^{T_s} \frac{2v_{in} - v_o}{n} dt\right) = 0 \tag{14}$$

equal to V_L:
Volt-second balance rule for the inductors is as follows:

$$M_{CCM} = \frac{v_o}{v_{in}} = \frac{d(n-2)+2}{1-d} \tag{15}$$

Using the mentioned relations, an ideal gain voltage for the

$$v_{D_{o2}} = -v_{Co2} = -\frac{d(n-1)+1}{1-d} \tag{16}$$

suggested converter under CCM will be as it follows:
The relation (13) is measured by relations (9) and (15):

$$v_s = v_{in}\left[-2\left(\frac{2}{n} - \frac{d(n-2)+2}{n(1-d)}\right)+1\right] \tag{17}$$

The voltage stress on switch S is obtained from the following relation:

$$i_L = \frac{1}{L}\left(\frac{2v_{in} - v_o}{n}\right)t + i_{L\max} \tag{18}$$

The current size of inductors in this time interval is attained from the following relation:
Now, we can measure the average output current I_o. Suppose that the capacity of the output capacitor is high such that fixed voltages in both sides are obtained. Therefore, the average

$$I_o = \bar{i}_{d_{02}} \tag{19}$$

current of the output capacitor is zero because the voltage is continuous, i.e.
where $\bar{i}_{D_{02}}$ is the average current of diode D_{o2}. It passes the

$$i_{d_{o2}} = i_L \tag{20}$$

current only in the second time interval, and has a current equal to the inductor current, i.e.

$$I_o = \frac{1}{T_s}\int_{(1-d)T_s}^{T_s} \frac{1}{L}\left(\frac{2v_{in} - v_o}{n}\right)t + i_{L\max} \tag{21}$$

$$I_o = \frac{1}{2}(1-d)(i_{L\max} + i_{L\min}) \tag{22}$$

After integrating on the whole time intervals, the average output current is obtained:
Function of Suggested Converter under DCM (Discontinuous Conduction Mode):
In this mode, the inductor current does not reach the maximum

mode CCM in the scope of size d of inductor current, and the energy saved in the inductor is zero before the end of the

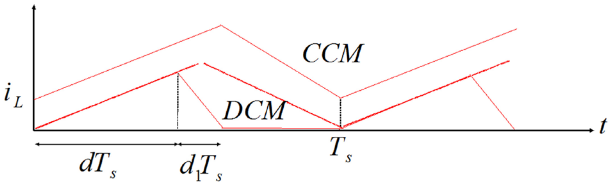


Fig. 7. Current i_L in Mode DCM.

second time interval. In this mode, i_{Lmin}=0. Figure 7 indicates the form of wave i_L in this mode and other modes to CCM. According to Figure 7, the voltage gained in this mode is obtained

$$M_{DCM} = \frac{v_o}{v_{in}} = \frac{nd + 2d_1}{d_1} \tag{23}$$

using the relations of the inductor voltage in the first and second time intervals and average formula in shown equation 23. The average current of the output capacitor is zero;

$$I_{co} = \frac{\frac{1}{2} d_1 T_s i_{L\max} - I_0 T_s}{T_s} \tag{24}$$

hence, the figure 8 has been resulted from the following equation:

$$I_{co} = \frac{nd^2 T_s v_{in}}{2(M_{DCM} - 2)L} - I_0 \tag{25}$$

The following relations hold after the replacement of relations (23) and (7):

$$M_{DCM} = \frac{v_o}{v_{in}} = 1 + \sqrt{2 + \frac{nd^2}{\tau}} \tag{26}$$

Given (25) $\frac{Lf}{R}$ and that the gain voltage is equal to zero in this

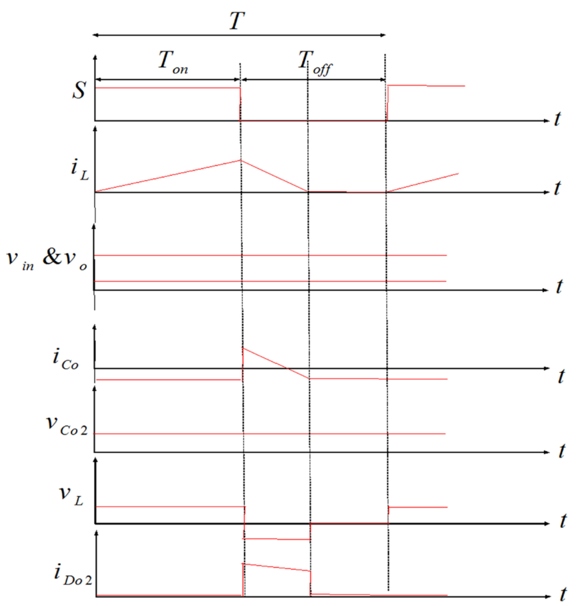


Fig. 8. Waves of DCM Mode

mode , this is obtained:
where .
Function of Suggested Converter under BCM (Boundary Conduction Mode)

$$I_o = \frac{1}{2}(1-d)(i_{L\max}) \tag{27}$$

In this mode, the inductor current reaches zero; i.e. i_{Lmin}=0.

$$i_{L\max} = \frac{1}{L} V_{in}(dT_s) \tag{28}$$

The relation (22) is simplified as follows:
i_{Lmax} is obtained from the relation (7) as:

$$I_o = \frac{d}{2Lf}(1-d)V_{in} \tag{29}$$

I_o is obtained according to d by inserting the relation (28) in relation (27):

$$I_o = \frac{d}{2Lf} \times \frac{(1-d)^2}{d(n-2)+2} V_o \tag{30}$$

The equation (25) is revised as follows according to output voltage:

$$\tau \geq \frac{d}{2} \times \frac{(1-d)^2}{d(n-2)+2} \tag{31}$$

$$f(d) = \frac{d}{2} \times \frac{(1-d)^2}{d(n-2)+2} \tag{32}$$

The relation (31) is obtained because I_o in the mode CCM is larger than I_o in boundary mode:
Figure 9 shows f(d) according to (n=2). If τ is larger than f(d), the converter function is placed in the mode CCM as per d but it is impossible in practice because induction or frequency shall be large in this case. See Figure 9. The charge line crosses τ in two points and establishes three zones. The

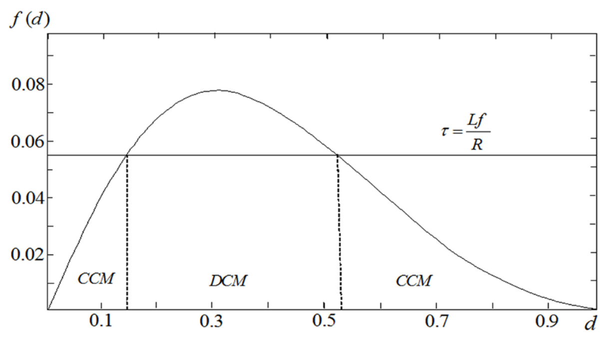


Fig. 9. Diagram f(d) with respect to d

middle zone of the converter function is under mode DCM and the other two zones in CCM.

4- Simulation results in mode ccm:

To study the accuracy of the converter function, a circuit with specifications mentioned in Table 1 has been simulated with the help of PSCAD/EMTDC. Given n=3, the inductor block includes three inductors and six diodes as output voltage increases to 500V by regarding d=50% (Figure 10) . Figure 12 shows current ripple ic2 which is very low. The inductors placed in the inductor block have the same charge and discharge currents and forms of wave i_{L1}. Figure 12 indicates

Table 1. Circuit parameters for simulation

V_{in}	100V	P_o	2.5KW	L_1	400µH
f_s	10KH	n	3	L_2	400µH
d	50%	R_o	100Ω	L_3	400µH
C_1	100µF	C_2	100µF	L_o	400µH
C_3	100µF		C_0		100µF

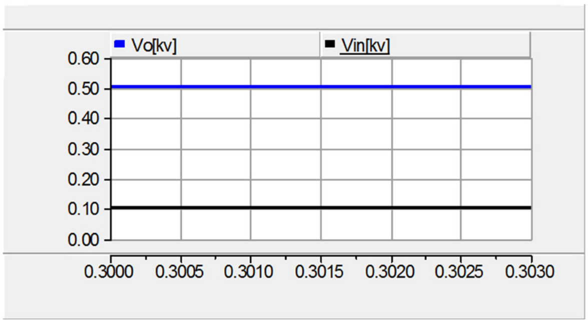


Fig. 11. The Vout and Vin (Time Horizental Line [s])

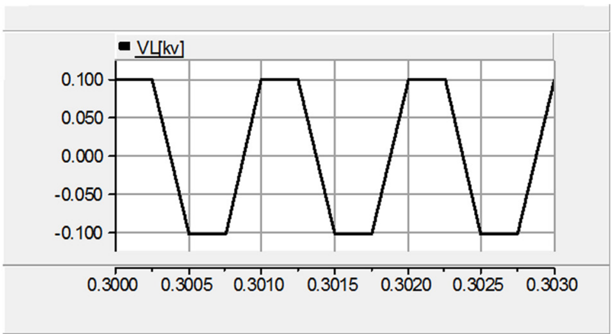


Fig. 12. Voltage Wave V_{L_1} (Time Horizental Line [s])

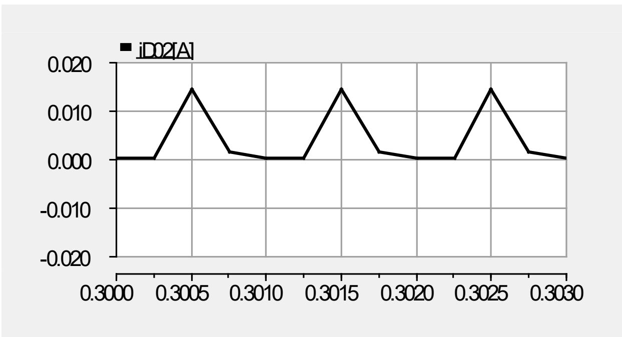


Fig. 13. Current Wave i_{DO2} (Time Horizental Line [s])

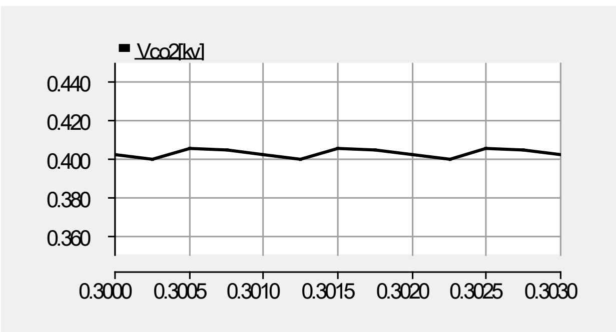


Fig. 14. Voltage Wave v_{co2}(Time Horizental Line [s])

v_{L1}, and the way of turning on and off D_{o2} is presented in Figure 13. Also, Figure 14 indicates the ripple of voltage C_{o2}.

5- Comparison of suggested converter with converters [3] and [12]:

Table 2 presents a comparison of converters analyzed in [3] and [12] with the suggested converter. For example, in performance

Table 2. Comparison of suggested converter with converters in [3] and [12]

duty cycle d=72.7%	Voltage Gain $\frac{V_o}{V_{in}}$	voltage stress on switch	Switch number
[12]	7.33	$3.66 \times V_{in}$	2
[3]	8.33	$3.66 \times V_{in}$	1
Suggested Converter: n=3	10	$3.34 \times V_{in}$	1

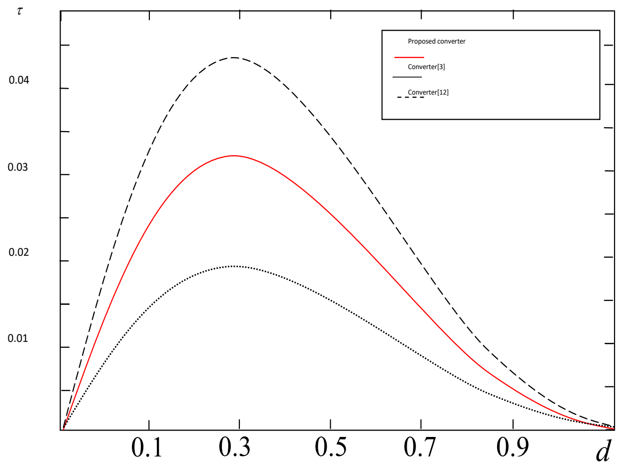


Fig. 15. Diagram τ According to d

period d=72.7%, the voltage gain of suggested converter was 10, and the voltage stress on switch was reduced.

Figure 15 shows diagram t with respect to the d. As shown, the suggested converter has proper performance in CCM mode.

6- CONCLUSION

The simple structure of the suggested converter is able to increase the voltage by the inductive switching block and the combination of capacitor and diode. Also, a higher voltage would be achieved by adding diode inductive levels. This converter has fewer elements than the converter in [12]. Moreover, a high voltage gain will be obtained by placing a source into the circuit in two states of switching. Because of the capacitors, in series with the switch, voltage stress on the switch decreases and the existence of serial inductors with output capacitor will reduce the output voltage ripple. Conduction mode is a bit greater in CCM. The output voltage may increase by 120V (d=72.7% , n=3) for a PV system with output electricity 12 V by installing this converter. Finally, this paper analyzed the converter function in continuous, discontinuous, and boundary modes. The voltages and currents of some

References

[1] W.-Y. Choi, J.-S. Yoo, J.-Y. Choi, High efficiency dc-dc converter with high step-up gain for low PV voltage sources, in: Power Electronics and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conference on, IEEE, 2011, pp. 1161-1163.

[2] Q. Zhao, F.C. Lee, High-efficiency, high step-up DC-DC converters, IEEE Transactions on Power Electronics, 18(1) (2003) 65-73.

[3] B. Wu, S. Li, S. Keyue, A new hybrid boosting converter, in: Energy Conversion Congress and Exposition (ECCE), 2014 IEEE, IEEE, 2014, pp. 3349-3354.

[4] M. Prudente, L.L. Pfitscher, G. Emmendoerfer, E.F. Romaneli, R. Gules, Voltage multiplier cells applied to non-isolated DC–DC converters, IEEE Transactions on Power Electronics, 23(2) (2008) 871-887.

[5] S. Lee, P. Kim, S. Choi, High step-up soft-switched converters using voltage multiplier cells, IEEE Transactions on Power Electronics, 28(7) (2013) 3379-3387.

[6] J.C. Rosas-Caro, J.M. Ramirez, F.Z. Peng, A. Valderrabano, A DC–DC multilevel boost converter, IET Power Electronics, 3(1) (2010) 129-137.

[7] F.L. Luo, H. Ye, Positive output multiple-lift push-pull switched-capacitor Luo-converters, IEEE transactions on industrial electronics, 51(3) (2004) 594-602.

[8] J.A. Starzyk, Y.-W. Jan, F. Qiu, A DC-DC charge pump design based on voltage doublers, IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, 48(3) (2001) 350-359.

[9] F.L. Luo, H. Ye, Positive output super-lift converters, IEEE Transactions on Power Electronics, 18(1) (2003) 105-113.

[10] N. Vazquez, L. Estrada, C. Hernandez, E. Rodriguez, The tapped-inductor boost converter, in: Industrial Electronics, 2007. ISIE 2007. IEEE International Symposium on, IEEE, 2007, pp. 538-543.

[11] T.-F. Wu, Y.-S. Lai, J.-C. Hung, Y.-M. Chen, Boost converter with coupled inductors and buck–boost type of active clamp, IEEE Transactions on Industrial Electronics, 55(1) (2008) 154-162.

[12] L.-S. Yang, T.-J. Liang, J.-F. Chen, Transformerless DC–DC converters with high step-up voltage gain, IEEE Transactions on Industrial Electronics, 56(8) (2009) 3144-3152.

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