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that are sorted in one-time frame which begins from one primary input and ends directly in one primary output. Our results indicate that all fault coverage values are higher than %85, while the numbers of test vectors are very low.

Table (1) Experimental Result for several asynchronous circuits.

Circuit name	No. of inputs/ output	No.of global feedback	Total path	No. of test vector	No. of RTP	No. of CTP	No. of UTP	Fault coverage
Atod	3/3	10	14	3	7	5	2	%85.7
Converta	2/3	17	77	9	53	16	8	%89.7
Ebergen	2/3	8	34	5	21	8	5	%85.3
Hazard	2/2	4	20	4	9	8	3	%85
Nowick	3/3	4	13	3	9	4	1	%92.4

7- Conclusion

In the previous works, inspection of paths for delay faults test has been done for each path. A path begins from a flip-flop or primary input and ends in a flip-flop or primary output Since the delay fault of each path segment is inspected individually and the applied input may pass through several path segments and the accumulation of delays of the path segments may become more than the threshold, it is possible that the path to be faulty. However, the fault remains un-inspected. In this paper a path is considered as one piece which begins with a primary input and ends with a primary output. Each path contains one or more path segments.

Since in previous papers the two applied test vectors to the circuit for delay faults test were not considered simultaneously, some paths could be considered as UTP while they were not, or the CTP paths might be mistakenly considered as RTP. In this paper, distinguishing the path types of a circuit for delay fault tests is done by simultaneous consideration of the two test vectors. As a result the paths are settled in only one of the three groups RTP, UTP, and CTP.

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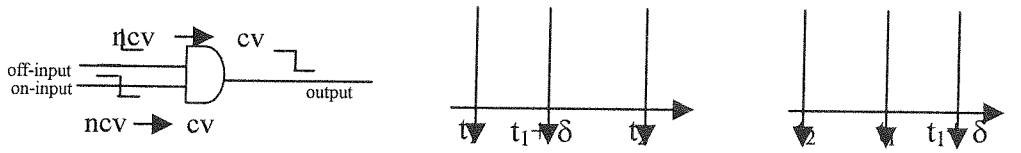
is detectable. This state for an AND gate is shown in Figure 6-a. Assume that on-input transition and off input transition take place at the time t_1 and t_2 respectively, and $t_1 < t_2$. If the delay fault is equal to δ at on-input (Figure 6-b), then the delay fault makes the transition to occur at the moment $t_1+\delta$. In this situation, the fault is detectable and the path p is testable. However, when $t_1 > t_2$ (Figure 6-c), the transition reaches the output before the time $t_1 + \delta$ through the off-input, the delay fault on on-input is not detectable and the path is not testable.



a: transition for AND gate b: timing in output $t_1<t_2$ c: timing in output $t_1>t_2$

Figure (6) condition for theorem 5-3 in AND gate.

5-3-1-Result

In a circuit, where the following conditions exist:

a- If there are two paths of p_1 and p_2, with the same beginnings and endings and share a common gate (with an input from p_1 and another input from p_2)

b- If applying a test vectors $V=<v_1,v_2>$ result in a ncv → cv on both inputs of the common gate.

Then:

the delay fault of the path is only detectable on the shorter (in time) path that is the same as the one which propagates transition to the output.

An example of such a path is shown in figure 7. The two paths {a, b, c, d} and {a, d} have the same beginning, a, and the same ending, d. A falling transition on a, makes the gate g_3 to have two similar inputs ncv → cv. Thus either of the paths which do the transition faster is testable. This means that the path is a CTP.

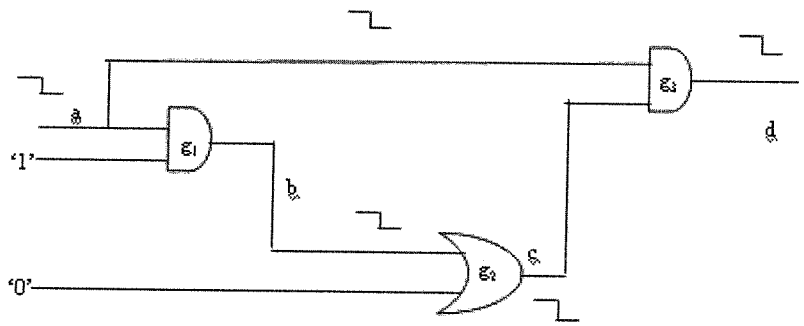


Figure (7) Two paths with the same start and end.

6-Experimental Results

A program in the C language is used to test the PDFs of the SIS benchmark asynchronous circuits. This program determines the type of the path, RTP, UTP, and CTP. According to this categorization, the UTP paths are distinguished and in view of that the fault coverage may be determined for the circuit.

Table 1 shows the experimental results for some SIS benchmark circuits. The number of paths in this table is the set of paths in one- and two-time frames. The paths that are ranked in two-time frames contain two-path segments (one path begins with a primary input and ends with a flip-flop, the other path begins with a flip-flop and ends with a primary output) and

Considering result 5-2-2, it may seem that the delay in each of the off-input or on-input of the gate may cause a 101 or 010 output. Hence output, which should have a 1 (or 0) value at any time, takes a 0 (or 1) value for a while [8]. However, this output shows a 0-hazard (1-hazard). Thus the condition of untestability of the path is not valid any more. Since the circuits are hazard free, such a condition may not occur in the output.

Figure (5) condition for result 5-2-2 in AND gate.

4-3-Conditional Testable Path (CTP) Distinguishing Theorem

If in the path p for the pair vectors $V=\langle v_1,v_2\rangle$, (a) the desired transition is observed in the output and (b) in the considered path at least once, both of the following conditions occur in one of the gates:

$$\exists\, g_{ij} \in p:\ \text{off-input } g_{ij}(v_1) = \text{on-input } g_{ij}(v_1) \qquad i\in\{0,..,n\} \tag{11}$$

$$\exists\, g_{ij} \in p:\ \text{off-input } g_{ij}(v_2) = \text{on-input } g_{ij}(v_2) \qquad i\in\{0,..,n\} \tag{12}$$

then the p is a CTP. The testability conditions may be divided into the following choices:

1-If transition of v_1 to v_2 on the inputs is cv $\rightarrow$ ncv then the condition of testability for path p is so that no other delay fault exists for the path p which causes a delay in off-input. Therefore, the fault is detectable and the path is testable.

2- Transition from v_1 to v_2 occurs in the form ncv $\rightarrow$ cv on the inputs. If in the path p the on-input transition propagation occurs earlier, the fault is detectable and the path is testable; otherwise the path is untestable.

Proof:

When conditions 11 and 12 are satisfied, the same transition takes place in both inputs. In the first choice of above mentioned testability condition, the transition from v_1 to v_2 is in the form cv $\rightarrow$ ncv. Therefore, if there is no delay in off-input during a specific time, the off-input changes to ncv and the output value is still determined by on-input, because it is in cv state. As a result, the delay of cv $\rightarrow$ ncv transition in on-input reaches directly to the output and the delay fault is propagated to the output, the delay fault is detectable, and thus the path is testable.

If the delay fault exists in off-input, with presence of the delay fault in the on-input path (which is lower than the delay fault in off-input), the transition will still take place earlier and thus on-input turns to ncv earlier. At this time, the output value is determined based on the off-input which has a cv value and no change is observed in the output due to the transition. After passing the delay time of the off-input, the change due to the transition is observed in the output; in other words, a delay equal to the off-input delay occurs in output and the delay due to fault in on-input is not observed on output.

For the second choice of the theorem, the transition from v_1 to v_2 is in the form of ncv $\rightarrow$ cv. Each of the inputs with an earlier transition causes transition propagation to the output. Therefore, if the off-input does the transition, with less delay with respect to the on-input, even if the on-input has delay fault, the delay fault in on-input can not be detected. This is because the considered transition is done through off-input. However if on-input, in a specific and shorter time as compared with the off-input, shows the transition on the output, the fault

2-The transition (falling or rising) changes are observed in the output. Since the on-input at least one time has had a constant value in the path p at gate g_{ij} then the transition propagation is reached to the output through off-input of gate g_{ij} or its subsequent gates (to the output). Therefore the transition propagation has not occurred through the considered path p. So the path p is a UTP. A UTP path {a, b, c, d} is shown in Figure 4.

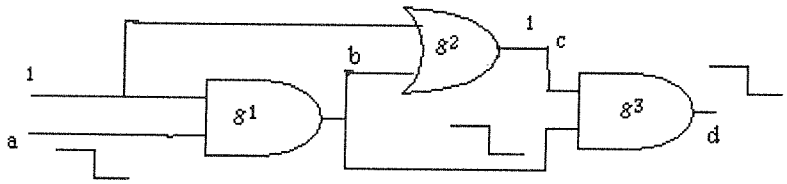


Figure (4) untestable path for falling transition.

4-2-1-Result

For the pair vectors $V=<v_1,v_2>$, if at least one off-input exists in the path p with the following condition:

(8) $\exists\, g_{ij} \in p$: off-input $g_{ij}(v_k)$ = stable cv $\quad i\in\{0,..,n\}, j\in\{0,..,m\}, \; k\in\{1,2\}$

then the path p for the pair vectors V is a UTP.

Proof:

When the condition of result 5-2-1 is satisfied, it makes the on-input $g_{i+1j}(v_k)$ to have a constant value for the pair vectors V. Therefore the transition does not reach the output through the path p. According to the condition of the theorem 5-2 when on-input $g_{i+1j}(v_k)$ has a constant value for v_1 and v_2, it is either in stable state cv or in stable state ncv. This indicates that the transition has not reached from on-input to the output of the gate g_{i+1j}. Therefore the off-input of the previous gate should not allow this transition propagation. This shows that the off-inputs $g_{ij}(v_k)$ have constant values for both v_1 and v_2 which are cv so as not to allow the transition propagation (Figure3).

4-2-2-Result

In a path p for gate g_{ij}, if one of the two following sets of conditions is satisfied, then the path p is a UTP

$$\begin{cases} \text{(off-input } g_{ij}(v_1)\text{=cv and off-input } g_{ij}(v_2)\text{= ncv)} & i\in\{0,..,n\}, j\in\{0,..,m\} \\ \text{(on-input } g_{ij}(v_1)\text{=ncv and on-input } g_{ij}(v_2)\text{= cv)} & i\in\{0,..,n\}, j\in\{0,..,m\} \end{cases} \quad (9)$$

and

or

$$\begin{cases} \text{(off-input } g_{ij}(v_1)\text{=ncv and off-input } g_{ij}(v_2)\text{= cv)} & i\in\{0,..,n\}, j\in\{0,..,m\} \\ \text{(on-input } g_{ij}(v_1)\text{=cv and on-input } g_{ij}(v_2)\text{= ncv)} & i\in\{0,..,n\}, j\in\{0,..,m\} \end{cases} \quad (10)$$

and

Proof:

If either of the two sets of conditions of the result 5-2-2 is satisfied for the path p, then the value of on-input g_{i+1j} would be a constant (stable cv or stable ncv). Therefore, according to the theorem 5-2 the path p is a UTP. The condition of result 5-2-2 are shown in Figure 5 for AND.

Assuming that for a sequential path p the condition (1) is satisfied, and then the off-inputs for the vectors v_1 and v_2 will always be stable ncv. By establishing condition (2), the transition will be propagated from the considered gate. This means that the propagation is done only in the main path p. This process is repeated for all of the existing g_{ij}'s in the path. Finally the transition would be entered into the output, the fault is detectable and the path is testable (Because for all the g_{ij}'s of the paths, both conditions (1) and (2) are satisfied.).

On the other hand, since the off-inputs have had no changes in the path and remained constant, if there is any delay fault in the paths of the circuit, it should go to the output through on-input of the path. However, by establishing condition (2) the transition comes to the output through the path p and the fault of this path is detectable. Therefore by this test pattern the path p is testable and it is an RTP.

4-1-1-Result

By applying a pair vectors V to a path p, if the following conditions are satisfied:

$\forall\, g_{ij} \in p$ off-input $g_{ij}(v_k)$ = stable ncv $\quad i\in\{0,..,n\}, j\in\{0,..,m\}, k\in\{1,2\}$

$\forall g_{ij} \in p$ on-input $g_{ij}(v_1) \neq$ on-input $g_{ij}(v_2)$ $\quad i\in\{0,..,n\}, j\in\{0,..,m\}$

If the off-inputs are stable cv then they will not allow the transition (falling or rising) to be propagated through the on-input of the path p, hence condition (6) is not satisfied. If both conditions (5) and (6) were satisfied, according to the above mentioned theorem, the path p would be an RTP for the pair vectors V.

4-2-UnTestable Paths (UTP) Distinguishing Theorem

For the pair vectors $V=\langle v_1, v_2\rangle$ in a path p, if the following condition is satisfied:

$\exists\, g_{ij} \in p$: on-input $g_{ij}(v_1)$ = on-input $g_{ij}(v_2)$ $\quad i\in\{0,..,n\}, j\in\{0,..,m\}$

Then path p for the pair vectors V is a UTP.

Proof:

Two different cases in path p may occur:

1-In the path p the condition of the theorem is satisfied. Since the changes only occur in primary input (falling or rising transition), after the gate g_{ij} values on all of the on-inputs of the subsequent gates along the path, from g_{ij} to the primary output will be constant. No transition in the path p reaches to the output. Therefore the path p for pair vectors V is a UTP.

A UTP path {a, b, c, d} is shown in Figure 3. In this path on-input $g_2(v_k)$ = stable cv ('1') and on-input $g_3(v_k)$ = stable cv ('1') $k\in\{1, 2\}$. Therefore the path {a, b, c, d} is a UTP.

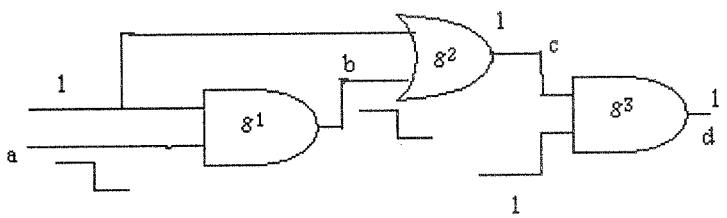


Figure (3) a UTP {a, b, c, d}.

v_1 can have different values (i.e. cv and ncv). In an asynchronous circuit the values of the inputs to each gate should be evaluated after stabilization. Therefore for each input (off-input and on-input) the two following cases occur:

off-input	on-input
cv or ncv	cv or ncv

Similarly, when applying vector v_2, each of the two inputs may be cv or ncv. In the process of transition of values, when vector v_2 is applied followed by vector v_1, one of the following transition cases may happen:

on-input or off-input: $v_1 \rightarrow v_2$
cv → cv
cv → ncv
ncv → ncv
ncv → cv

The first and third rows of the above table show that the inputs remain at a stable state of cv or ncv for each of the two vectors v_1 and v_2. In the inspected circuits each gate is considered to have at most two inputs and each input may have a maximum of four states. Therefore by applying the vectors v_1 and v_2 for each gate 16 (4^2) different states may occur for each pair of inputs. Increasing the number of the inputs to the gate raises the possible states for each gate. In other words, for each gate with k inputs, 4^k different states may occur.

4-New Theorems for Path Delay Faults Categorization

Three new theorems are presented in this paper to categorize PDFs. In these theorems g_{ij} denotes the i^{th} gate for j^{th} frame. In addition, the input value of the gate g_{ij} for an off-input in return for the input vector v_k is shown by "off-input g_{ij} (v_k) ". Furthermore, the input value of the gate g_{ij} for an on-input in return for the input vector v_k is shown by "on-input g_{ij} (v_k) ". All theorems apply a pair of test vectors $V=<v_1, v_2>$ to the circuit. It is assumed that the vectors v_1 and v_2 are different by only one input (one bit) that is a primary input to the path p.

4-1-Robust Testable Paths (RTP) Distinguishing Theorem

For the pair vectors $V=<v_1, v_2>$, if the desired transition (falling or rising) on the path p is observed in the output and for all the gates of the considered path, the following conditions are satisfied:

$$\forall g_{ij} \in p \quad \text{off-input } g_{ij}(v_1) = \text{off-input } g_{ij}(v_2) \qquad i \in \{0,..,n\}, j \in \{0,..,m\} \tag{1}$$

$$\forall g_{ij} \in p \quad \text{on-input } g_{ij}(v_1) \neq \text{on-input } g_{ij}(v_2) \qquad i \in \{0,..,n\}, j \in \{0,..,m\} \tag{2}$$

The pair of vectors V is a test pattern for the path p and it robustly tests the path p. The path p is inherently an RTP.

Proof:

The above mentioned conditions show that, in the considered path, the off-inputs should have ncv values to allow the transition (falling or rising) propagate from on-input. Therefore the value of off-input is a stable ncv and the on-inputs cover one of the two following situations:

ncv → cv
cv → ncv

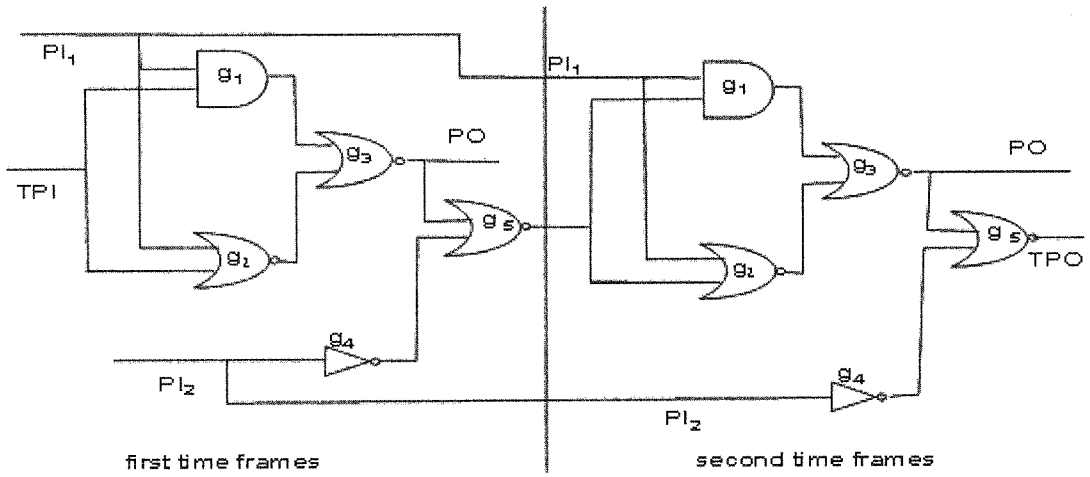


Figure (2) an asynchronous circuit in two time frames.

2-PDFs Categorization

Based on the delay faults in each path of the circuit, a new categorization of the paths is established in which three categories are considered as follows:

a: Robust Testable Paths (RTP)

In this category the paths are testable without any condition. By applying the pair of test vectors V=<v_1, v_2>, despite the existence of other delay faults in the other paths, the path can still be tested.

b: UnTestable Paths (UTP)

In this category the paths are untestable under any condition. Untestability of these paths is in two different forms:

1-There is no rising or falling transition on the path. Therefore by applying a pair of vectors V=<v_1, v2> as the input of the circuit, the output value, for both vectors v_1 and v_2, always appears as 0(or 1)

2-The desired rising or falling transition may occur on the considered path but before the appearance of the transition affects in the output, the effect of the transition may appear in the output through a faster path (within a shorter period of time). When there are two paths with common starts and ends this condition may happen. A transition in the input may propagate through two different paths and the results of this propagation finally come together in an output.

c: Conditional Testable paths (CTP)

In this category the paths are testable under specific conditions which will be discussed later.

3-Simultaneous Inspection of the Test Vectors

When a pair of vectors V is applied to identify PDF in a circuit, if the output of v_1 and v_2 are not identical, the two vectors may be used as a pair of test vectors. Error arises with the traditional categorization, when it is necessary to evaluate the state of the vectors simultaneously. For example for an AND gate with two inputs of 'a' and 'b' and applied test vectors of v_1 = <a=0,b=x> (x = don't care) and v_2 =<a=1,b=1> the path to the output is a robust testable path [4]. However, it is possible that the path under the input x=0 is not robust testable. If the delay fault is in input 'b' the effect of 0 value (caused by 'b') may be the result of output at the sampling time. Therefore this is a conditional testable path. While in the existing categorizations, this path can be classified in both testable and untestable categories. Because of such errors, it is important to evaluate both vectors simultaneously.

In a gate with two inputs of 'a' and 'b', each input value of the gate, when applying vector

circuits is presented as follows:

* An asynchronous circuit is considered to be an asynchronous network where a path is defined as: $P= \{g_{00}, g_{01},\ldots, g_{ij},\ldots g_{mn}\}$.

Where i is the number of time frame repetitions for each input, $0 \leq i \leq m$, and j is the number of gates in a path at each time frame, $0 \leq j \leq n$. According to this definition, a path begins from a primary input and ends at a primary output. When an input value is applied to the circuit until the stabilization of its effect at the primary output, it may pass through several feedbacks of the main asynchronous circuit. A gate may be repeated several times in a path. The maximum number of a gate repetition is equal to the maximum time frames of the circuit until an input value is finally propagated to the primary output.

Figure 1 indicates an example of an asynchronous circuit in which, to determine the output value in return for the input (PI_1=1, PI_2=0), the circuit may be analyzed as follows:

At the beginning instant the output of the flip-flop has an undetermined value 'U', therefore output value of the gate g_1 is also undetermined while the output of the gate g_2 is equal to '0'. Thus the output of gate g_3, which is the same as the primary output, is the undetermined value 'U'. The output of gate g_4 is '1' and the output of gate g_5 is '0'. Therefore in the first time frame, primary output has yet an undetermined value and the second time frame should also be passed until the output value becomes stable. At this time the outputs of gates g_1 and g_2 are equal to '0', the output of gate g_3 is '1' and finally the output of gate g_5 is equal to '0'. Therefore after the second time frames the effect of the input vector 10 causes a stable value '1', in the output. Thus the circuit of Figure 1 may be shown in the form of Figure 2.

In Figure 2 the temporary primary input (TPI) is the cut-off feedback of the circuit and its value for the primary inputs is 'U' at the first time frame. The temporary primary output (TPO) is the cut-off feedback in the circuit. In this circuit, merely, the global feedback is cut. A sample for the paths in this circuit is:

$$p: g_{01}, g_{03}, g_{05}, g_{11}, g_{13}$$

where g_{01}, g_{03} and g_{05} appear at the first time frame, and g_{11} and g_{13} at the second time frame in the path. g_{01} and g_{11} are the same as gate g_1 which is considered in two different time frames.

It is to be noted that the number of the time frames could be increased or decreased for the inputs other than 10. According to the example in figure 1, the path p itself contains two path segments: p_1: g_{01}, g_{03}, g_{05} and p2: g_{11}, g_{13}.

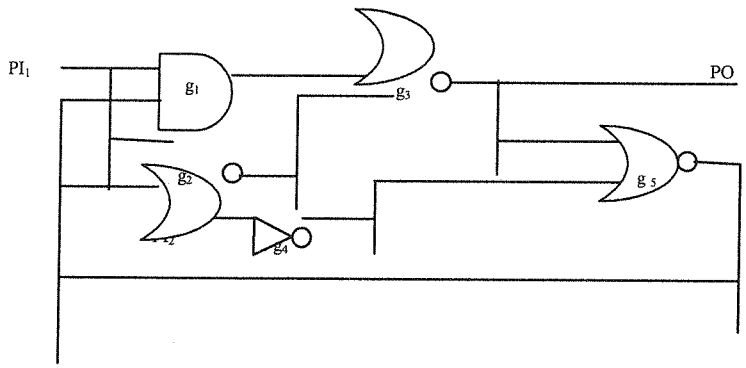


Figure (1) an asynchronous circuit in one time frame.

It is possible that paths p_1 and p_2 have small delays, less than the acceptable threshold. Hence both paths are considered to be without any fault, but the accumulation of the delays in p_1 and p_2, which appear in the path p, may pass the threshold. Therefore, despite of p_1 and p_2 being without fault, p is a faulty path.

it is called a robust test. Otherwise it is a non-robust test.
* A path p is static sensitizable for a transition (falling or rising) if, for each gate g belonging to the path p, every off-input has a ncv. Otherwise it is a static unsensitizable path. [9]
* A path p is functional sensitizable for a transition (falling or rising) if, for each gate belonging to the path p, every off-input has a ncv, whenever the on-input of that gate has a ncv. Otherwise it is functional unsensitizable. [9]

In the following study, paths of asynchronous circuits are also categorized based on the same above-mentioned definitions.

However, other classifications are introduced by Lam *et al (1995)*, Cheng and Chen (1996), Gharaybeh *et al.* (1997), Sivaraman and Strojwas (1997), Kristic *et al.*

Lam *et al (1995)*, classified PDFs in two groups of robust dependent (RD) and non-RD, where non-RD delay faults are not required to be tested if all RD faults have been tested [10]. Cheng and Chen (1996) classified PDFs in four groups of robust testable, non-robust testable (similar to static sensitizable), functional sensitizable, and redundant (the paths which never become sensitized) [23]. Gharaybeh *et al.* (1997) categorized PDFs in three groups of single testable (similar to robust and non-robust), singly testable dependent (in which the transition is not propagated), and the multiply testable [12]. Sivaraman and Strojwas (1997) also introduced a new categorization where PDFs are divided into three groups, primitive Single Path Delay Faults (SPDF), primitive Multiple Path Delay Faults (MPDF), and primitive dependents [24].

These categorizations are introduced for the combinational circuits that are used for sequential circuits in some cases. For sequential circuits, Kristic *et al.* classified PDFs in three categories of testable PDFC, testable PDFC, and UnTestable [9]. All of these categorizations are created when applying a pair of test vectors $V=<v_1, v_2>$ to a circuit, while conditions of v_1, v_2 are evaluated separately.

The purpose of this study is to identify some difficulties associated with the test of sequential circuits. Furthermore, we propose a new theorem for testing of asynchronous circuits and evaluate the theorem by some examples. In our tests, we only considered PDFs and introduced a new definition for paths. In the categorization that is presented in this paper, the pair of test vectors is evaluated simultaneously.

1-The New Definition of Path in Asynchronous Circuits

A path begins from a flip-flop or primary input and ends at a flip-flop or primary output. In this study, we refer to path as path segments. If the delay time of a path does not exceed a specific limit (the threshold), then it will be assumed as a path without fault. According to this definition the delay of each path segment is tested individually. In an asynchronous circuit, because of feedback, the effect of input changes may pass through several path segments before becoming stable at the output. If each path segment is tested individually, its delay may be acceptable. However, in this case the accumulation of the path segment delays may cause a large and unacceptable delay at output. Therefore, the path may need to be defined in an alternative form for asynchronous circuits. In order to define such a path the following definitions are used:
* Global feedback is a feedback loop, which is closed through a gate. Therefore, a global feedback can connect one gate to another. The local feedback is a feedback loop that is closed inside flip-flop or C-element [7].
* An asynchronous network refers to an asynchronous circuit with no global feedback which is in the form of a combinational circuit containing some logical gates (NOT, AND, OR, NAND and NOR) and C-elements. In an asynchronous network the input of each gate is directly obtained from the output of another gate or a primary input [7].

On the basis of the above definitions, a new definition for a path in the asynchronous

Path Delay Faults Categorization in Asynchronous Circuits

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Abstract

Path delay fault models are introduced to diagnose failures that cause sequential circuits malfunction and violate timing specifications. For delay faults tests, a pair of test vectors is used for each path to be tested. Diagnosis of failure in asynchronous circuits is more important since the delay faults can change the function of the circuit. .However, asynchronous circuits and their faults are yet to be understood. The purpose of this study is to first identify whether the existing paths will accurately measure delays. Furthermore, a new definition for paths is introduced, which leads to a new category of path delay faults. This new category is different from previously proposed categories by suggesting simultaneous evaluation of pair vectors. Finally, the experimental results for SIS benchmark circuits are shown and the fault coverage is calculated for each circuit.

Keywords

Asynchronous Circuit, Path Delay Fault, Test vector.

Introduction:

A well known advantage of asynchronous circuits over synchronous circuits is that asynchronous circuits do not require global clock. It has been shown that such advantage provides less power consumption and higher performance [3, 15, 19]. Instead, asynchronous circuits require extra controllers. These controllers usually make the system more cumbersome and difficult to test [6, 15, 22].

By increasing the speed of systems operation, in addition to testing the system functional faults (e.g. s-a-v), it is necessary to test system performance faults (delay faults) as well. In synchronous circuits, the delay faults may decrease the circuit performance while in asynchronous circuits; the delay faults are capable of changing the function of the circuit [13, 22]. Depending on creation of delay on gate or path, delay faults are categorized in two groups of Path Delay Faults (PDF) and Gate Delay Faults (GDF) [2, 6, 10, 16, 17, 20, 22]. In GDF, delays are studied in one or more gates whereas in PDF delays are studied on the path [1, 11, 20, 21]. It is shown that a small delay fault my not be recognizable by GDF if the related gate is located on a path with low delay [20]. In contrast, in the PDF the delay is considered to be distributed on the path (the GDF are a sub-set of PDF [14]). Therefore, PDFs are more appropriate for testing of delay faults, because they model a larger set of faults [16, 18]. A path begins from a flip-flop or primary input and ends in a flip-flop or primary output. For delay faults test, a pair of test vectors $V = \langle v_1, v2 \rangle$ should be used for each path [5, 8].

Paths are categorized differently for the sequential and combinational circuits based on the following definitions:

* For each gate g in the path p if r is an input for the gate g and r is not in the path p then it is an off-input and if r is in the path p is an on-input.
* If the output value of the gate g with r input is determined by the r value, it is called a controlling value (cv) input and if the output value is not determined by the input r value, it is a non-controlling value (ncv) input.
* If a pair of test vectors distinguish path delay fault, apart from the existence of other faults,