AUT Journal of Modeling and Simulation

AUT J. Model. Simul., 50(2) (2018) 195-202
DOI: 10.22060/miscj.2018.13414.5072

Non-linear modeling, analysis, design and simulation of a solid state power amplifier based on GaN technology for Ku band microwave application

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ABSTRACT: In this paper, a non-linear approach for design and analysis of solid-state power amplifiers is presented and used for AlGaN-GaN high electron-mobility transistor (HEMTs) on SiC substrate for Ku band(12.4 - 13.6 GHz) applications. With combining the output power of 8 transistors, maximum output power of 46.3 dBm (42.6 W), PAE of 43% and linear gain of 22.9 dB were achieved and good agreement has been obtained between the simulation and analysis results.

Review History:

Received: 12 September 2017
Revised: 28 April 2018
Accepted: 17 June 2018
Available Online: 27 June 2018

Keywords:
Non-linear GaN modeling
power amplifier
Ku band
harmonic balance

1- introduction

The use of solid-state power amplifiers (SSPAs) in many radio communication systems, such as Ku band satellite communication systems, mobile cellular phone systems, etc., has significantly increased in recent years. The higher reliability of SSPAs, smaller size, and enhanced performance have resulted in an increased popularity over its traveling wave tube amplifier (TWTA) counterparts. AlGaN/GaN HEMTs have attracted much commercial interest due to the inherent advantages of their high voltage and high power density. Up to 8.1 W/mm pulsed power has been demonstrated from a 3.6-mm gate periphery device at 8 GHz [1]. 7.7 W/mm pulsed power has also been demonstrated at 35 GHz from standard 4 × 65-μm T-gated AlGaN/GaN HEMT [2]. Two kinds of high-efficiency power amplifiers (PAs) at X (30W and 60% PAE) and Ku bands (33% PAE, 100W) utilizing 0.15 μm GaN HEMT technology are presented at [3]. 16APSK data transmission has been done for Ku band satellite broadcastings with a 100 W class SSPA with very high linearity [4].

However, for high-power operation with a large gate periphery HEMT in the Ku band and other higher frequencies, many difficulties appear. For example, with the increase of device gate periphery, the device's impedance decreases steadily in proportion to the total gate width, which makes the external matching network design very difficult. As the chip's width has the same order as the micro-strips in the matching circuits, it becomes difficult to feed a microwave signal uniformly to such a large transistor [5]. The parasitic effects of the connection wire and the encapsulation shell are also significant at high frequencies. In addition, the self-heating effect and the defect trapping effect in the large gate periphery devices will both be more profound [6], [7] . These problems have prevented the easy development of large gate periphery HEMTs for high power operation with external matching circuits at high microwave frequencies. In this paper, a power amplifier with maximum output power of 46.3 dBm (42.6 W), PAE of 43% and linear gain of 22.9 dB is designed and simulated with harmonic balance analysis and a new fast algorithm instead of source pulling and load pulling. With presented design approach, power amplifiers are designed over frequency bandwidth and different input powers, which was over a single input power and single frequency in source pull and load pull algorithm. Designing for different input powers makes it possible for using in amplitude varying modulations.

In section 2, a parametric model of a GaN HEMT transistor is used for harmonic balance. Implemented harmonic balance is tested for some known scenarios and results verify parametric model, extracted parameters of model, and implemented harmonic balance algorithm. In section 3, a new design scheme is presented and a single transistor amplifier designed. Output power of 8 single transistor amplifier is combined to achieve desired output power.

2- GaN HEMT transistor

GaN HEMT transistors have higher break-down voltage, current density and electron mobility with respect to other combinations; thus, electrical current and output powers are increased [8]. Thermal resistivity is low and maximum tolerable temperature is high in GaN. This makes cooling system easier and cheaper. Maximum operating frequency in GaN transistor is high, and this makes GaN transistors suitable for generating power in microwave and mm-wave bands. These benefits are measured with some figure of merits, namely Johnson's and Baliga's figure of merits. As shown in [8], GaN HEMT is best choice.

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2- 1- Transistor model

In this paper, a temperature-dependent large-signal model for AlGaN-GaN high electron-mobility transistors (HEMTs) is chosen [9]. This model includes thermal, RF dispersion and bias-dependent capacitance model elements, which is suitable for harmonic-balance simulator. Large-signal model topology is shown in Fig. 1. The thermal model has a current source I_{th}, a resistance R_{th} ($^{\circ}C/W$), and a capacitance C_{th}. With these elements at a particular bias point, the device channel temperature T can be determined.

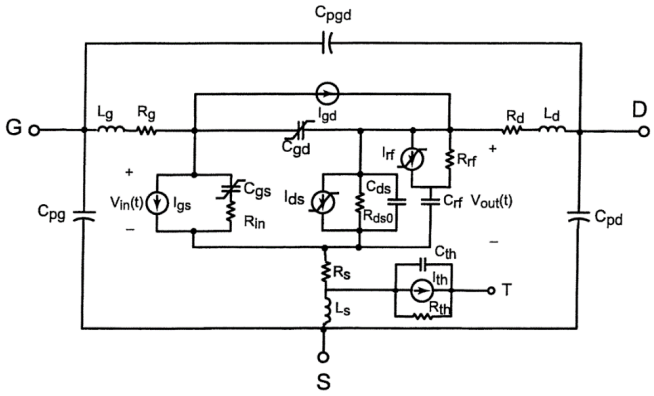

Fig. 1. Large-signal equivalent circuit with additional RF current source and output conductance branches are used to account for dc-RF dispersion.

The drain current model (I_{ds} in Fig. 1) is based on Curtice cubic model with temperature-dependent coefficients and internal time delay of FET [9 , 10]. The current source I_{th} in Fig. 1 is numerically equal to the instantaneous power dissipated in FET, and the $R_{th}C_{th}$ ($=\tau_{th}$) product is the thermal time constant. Package temperature $\tilde{T}$ can be determined by [9]:

$$\tilde{T} = R_{th}V_{ds}I_{ds} + T_0, \quad (1)$$

Where T_0 is ambient temperature and channel temperature T is determined by [9]:

$$T = [\frac{\tilde{T} - b(\tilde{T} - T_0)}{T_0^b}]^{1/1-b}. \quad (2)$$

With a model parameter $0 < b < 1$.

The non-linear behavior of the bias-dependent gate-source capacitance is modeled using [11],

$$C_{gs}(V_{in}, V_{out}, T) = C_{gs}(T)(\frac{1+c_{v1}V_{out}}{1+c_{v1}V_{ds0}})(\frac{1+f_{c1}\tanh[f_{c2}(V_{in}+v_{fcg})]}{1+f_{c1}\tanh[f_{c2}(V_{gs0}+v_{fcg})]}). \quad (3)$$

Where linearized temperature-dependent capacitance between gate and source is $C_{gs}(T) = C_{gs} + c_{gsT}\Delta T$ with $\Delta T = T - T_0$, the difference between the device channel and room temperature, and c_{gsT} is the temperature coefficient, V_{ds0} and V_{gs0} are the bias voltages used for C_{gs} extraction at room temperatures, and f_{c1}, f_{c2}, c_{v1}, and v_{fcg} are fitting parameters.

For gate-drain capacitance, we use the following equation,

$$C_{gd}(V_{in}, V_{out}, T) = C_{gd}(T)(\frac{1+c_{v2}V_{in}^2}{1+c_{v2}V_{gs0}^2})(\frac{1-f_{c3}\tanh(f_{c4}V_{out})}{1-f_{c3}\tanh(f_{c4}V_{ds0})}), \quad (4)$$

with $C_{gd}(T) = C_{gd} + c_{gdT}\Delta T$ where c_{gdT} is the temperature coefficient, and f_{c3}, f_{c4}, and c_{v2} are fitting parameters.

2- 2- Transistor model parameter extraction

The device epi-layer, fabrication, and RF testing results for AlGaN-GaN HEMTs used in this study have been previously introduced in [9], [12]. Two devices having different peripheries with a manifold gate finger arrangement were characterized, a 0.25 mm ($2\times125\mu m$) and a 1.5 mm ($12\times125\mu m$) device, both of which had a 0.35-μm gate length, a 3.0-μm gatedrain spacing, and a 1.0-μm gate-source spacing. The 1.5-mm device had substrate via-holes on the sources. The surface of the device was passivated by Si_3N_4. These devices had a maximum of approximately 600-mA/mm dc drain current and its pinchoff voltage was -4 V.

Pulsed I-V measurements were performed in [9]. Parasitic elements in Fig. 1 were determined by using a frequency-dependent fit [13] with measured S-parameters at cold-FET conditions. The small-signal intrinsic parameters were extracted using analytical equations for the Y-parameters for an intrinsic linear device model after de-embedding the parasitic elements [9]. The bias-dependent capacitance model fitting parameters were extracted using a least mean square error fit to the S-parameter data measured at 80 bias points at various temperatures. For the extraction of the temperature-dependent coefficients $A_i(T)$, the dc IV measured at elevated ambient temperatures, and the sets of A_i extracted using a least mean square error fit to the measured IV. The drain current parameters, i.e. λ, β, and γ, were extracted by an optimized fit to the measured IV [9].

2- 3- Harmonic balance analysis

For non-linear applications as power amplifier and mixer design, non-linear analysis and simulation is essential. Harmonic balance is a powerful tool in time-frequency domain. For this analysis, two constraints must be satisfied. First, device dimensions must be small relative to shortest wave length. Second, circuit must be in steady state.

For harmonic balance analysis, first step is dividing circuit model to linear and non-linear part. In Fig. 2, this division is shown. Four non-linear elements are in non-linear part and five ports are assigned to them. Temperature circuit model is not shown in Fig. 2. After a HB analysis and calculating drain current, new temperature is calculated and iteratively they would converge. So, in each HB analysis, temperature is constant and will not change.

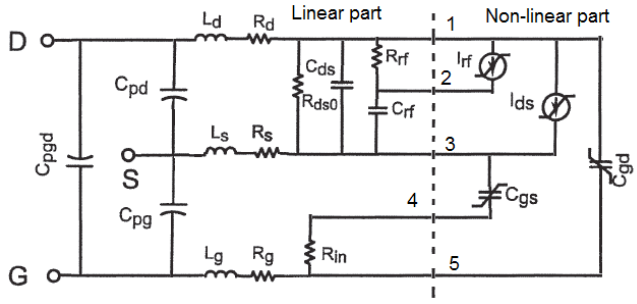

Fig. 2. Linear and non linear parts in circuit model of transistor.

Linear part is represented by a 7-port network. A 7-port Y-parameter is calculated for this network at required frequencies, using Agilent ADS [2009].

Non-linear current is calculated using equations introduced in [9]. Non-linear capacitances are calculated using (3) and (4),

and transformed to current after calculating the charge

$$Q(t)=C(V(t))\times V(t) \quad (5)$$

and a with a differentiation, currents of capacitance are:

$$I_c(t)=\frac{\partial Q(t)}{\partial t}. \quad (6)$$

This is easier in frequency domain as shown below:

$$I_c[k]=jk\omega_0 Q[k]. \quad (7)$$

After calculating currents of current sources I_{ds} in time domain, they are transformed to frequency domain and represented by Fourier series. Therefore, five-element current matrix of non-linear part at k'th harmonic is

$$I_{nlp}[k]=\begin{bmatrix} I_{rf}[k]+I_{ds}[k]+jk\,\omega_0 Q_{cgd}[k] \\ -I_{rf}[k] \\ -I_{ds}[k]+jk\,\omega_0 Q_{cgs}[k] \\ -jk\,\omega_0 Q_{cgs}[k] \\ -jk\,\omega_0 Q_{cgd}[k] \end{bmatrix} \quad (8)$$

2- 3- 1- Solving HB equation

HB equation is a KCL at linear and non-linear junctions. So it is

$$I_{nlp}+I_{lp}=0 \quad (9)$$

on any time if it is in time domain, or at any harmonic, if it is expressed in frequency domain. Non-linear currents can be calculated using (8) for a set of junction voltages. Linear currents can be calculated using Y-parameters, junction voltages and input voltages by

$$I_l[k]=\begin{bmatrix} I_{lp}[k] \\ I_6[k] \\ I_7[k] \end{bmatrix}=\begin{bmatrix} I_{1l}[k] \\ I_{2l}[k] \\ I_{3l}[k] \\ I_{4l}[k] \\ I_{5l}[k] \\ I_6[k] \\ I_7[k] \end{bmatrix}=Y_{7\times7}[k]\times\begin{bmatrix} V_1[k] \\ V_2[k] \\ V_3[k] \\ V_4[k] \\ V_5[k] \\ V_6[k] \\ V_7[k] \end{bmatrix} \quad (10)$$

In the above relation, I_l includes all linear currents, I_{lp} includes junction linear part currents, I_6 and I_7 are drain and gate (output and input) currents, respectively. $Y_{7\times7}$ is linear Y-parameters and V_i matrix represents voltages of all ports. For a given voltage, junction port currents can be written by

$$I_{lp}[k]=\begin{bmatrix} Y_{1,6}[k] & Y_{1,7}[k] \\ \vdots & \vdots \\ Y_{5,6}[k] & Y_{5,7}[k] \end{bmatrix}\begin{bmatrix} V_6[k] \\ V_7[k] \end{bmatrix}+\begin{bmatrix} Y_{1,1}[k] & \dots & Y_{1,5}[k] \\ \vdots & \ddots & \vdots \\ Y_{5,1}[k] & \dots & Y_{5,5}[k] \end{bmatrix}\begin{bmatrix} V_1[k] \\ \vdots \\ V_5[k] \end{bmatrix} \quad (11)$$

The first term is dependent on input voltage and is constant for DC term, because $V_6[0]$ and $V_7[0]$ are bias inputs and $V_7[1]$ is amplifier a constant input. Other harmonics of these two are zero. This constant matrix can be named $I_s[k]$ and (11) can be rewritten by

$$I_{lp}[k]=I_s[k]+Y_{5\times5}[k]\times V[k] \quad (12)$$

in which V [k] includes junction port voltages at k^{th} harmonics. Linear junction currents can be calculated using (12). Both linear and non-linear parts of current matrices are dependent on junction ports voltages. Goal of a HB analysis is to find a suitable junction port voltages matrix, that satisfies HB equation on (9). For solving this equation, optimization can be used. Newton-Raphson can also be used, but Jacobean matrix would be complicated because of complex non-linear modeling and numerous non-linear elements. Another method is separating method, which is done here. In this method, a guess of voltage matrix is made, then non-linear currents ($I_{nlp}[k]$) are calculated. The linear part's currents ($I_{lp}[k]$) are calculated using equation (9), and a better voltage approximation is made with rearranged equation (12)

$$V^{1}[k]=Y_{5\times5}[k]^{-1}\times(I_{lp}[k]-I_s[k]) \quad (13)$$

This can be done until voltages matrix is converged to a stable value ($V^N[k]$), then the analysis is finished and all voltages and currents are known.

For designing a power amplifier, a lot of bias points and matching impedances should be analysed. Changing matching impedance means changing Y-parameters matrices. In order to accelerate analysis, contribution of load and source impedances on Y-parameters are calculated and added to the equation (12) as it follows,

$$I_{lp}[k]=I_s[k]-I_s'[k]+(Y_{5\times5}[k]-Y_{5\times5}'[k])\times V[k] \quad (14)$$

I_s' and $Y_{5\times5}'$ are dependent on bias voltages, source, and load impedances at each harmonic. For an analysis, after selecting bias point, source, and load impedances, correcting values for

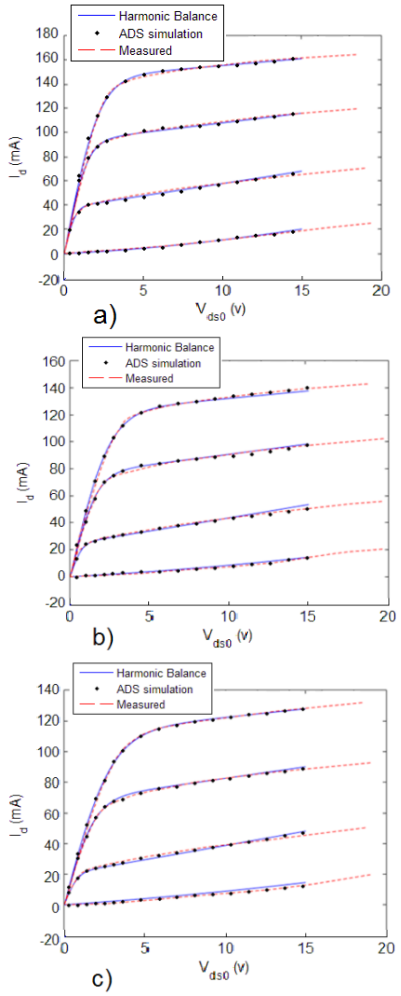

Fig. 3. DC I-V at : a) 27° b) 125° c) 200°.

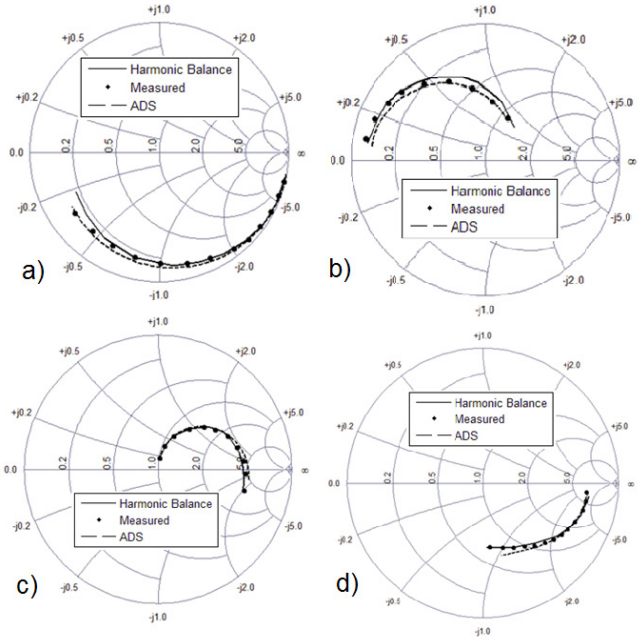

Fig. 4. S parameters results in simulation, analysis and measurements. a) S_{11} b) $S_{21}/5$ c) $S_{12}x5$ d) S_{22} .

I_s and $Y_{5\times5}$ should be calculated, and equation (14) is used instead of (12).

2- 3- 2- Verification of model and HB analysis with simulation and measurement

This harmonic balance algorithm is applied to some known problems, and results are compared to other simulators and measured data. All measured data are derived from [9].

DC operation results at some temperatures for 0.25 mm peripheries at V_{gs} from 0 to -3 V are shown in Fig. 3. Solid lines are harmonic balance analysis, dots are Agilent ADS harmonic balance result and dashed lines are measured data. Measurment process was performed in pulsed mode for restraining temperature at a constant value.

Small signal results for 1 to 26.5 GHz at 27° with V_{ds} = 15V and V_{gs} = -2V are shown in Fig. 4. In this figure, the solid lines are harmonic balance analysis, the dashed lines are Agilent ADS simulation and the dots indicates the measured data.

Large signal results from analysis and measurement for 1.5 mm periphery AlGaN-GaN with 50-ohm load and source impedances at 27° are shown in Fig. 5. In this scenario, V_{ds} = 20V , V_{gs} = -1.7V and input frequency was 8 GHz, which was not in Ku band, but measured data from [9] was at 8 GHz. The solid line and the dashed line are output power and gain, respectively, from analysis, and the dots represent the measured gain and the output power.

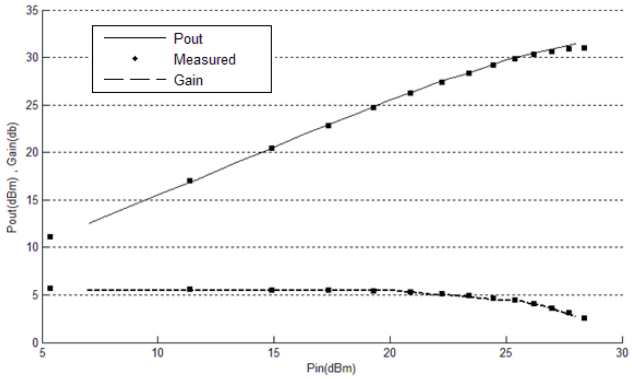

Fig. 5. Large signal analysis and measurement for 50-ohm load and source impedances.

3- Non-linear GaN power amplifier design

The above results show similarity among simulation, analysis and measurement. With this model, a 40 W power amplifier at Ku band is designed. Design procedure is explained in this section. 1.5 mm periphery AlGaN-GaN HEMT transistor which will be introduced later [9] is used for this design. Output power, linearity and power added efficiency (PAE), are three important characteristics for a power amplifier (PA). For designing a PA, source and load impedances and also bias points (gate-source and drain-source voltages) must be specified. PA's characteristics have non-linear dependency on these parameters and need a non-linear design. Firstly, a single transistor PA is non-linearly designed; then, their output power will be combined.

3- 1- Single transistor PA

Traditional PA design procedure was load pull, which was generating output power and PAE curves for a specific bias point, input power and source impedance over different load impedances and then selecting a suitable load impedance. This is done again over source impedance for selected load impedance, called source pull. These two steps are done iteratively to reach a better design.

This procedure can find suitable load and source impedances for a selected bias point and input power, but can not find suitable bias points, and can not consider linearity and neither bandwidth. New design procedure is presented here, which can consider linearity and bandwidth and also find suitable bias points.

3- 1- 1- Step 1: Linear approximation

PA is linearly designed and resulting bias point and source/load impedances are used as start point for next step. Resulting bias points are V_{ds0} = 31 V, V_{gs0} = -1.5 V, Z_S = 5 + j50 and Z_l = 50 + j20.

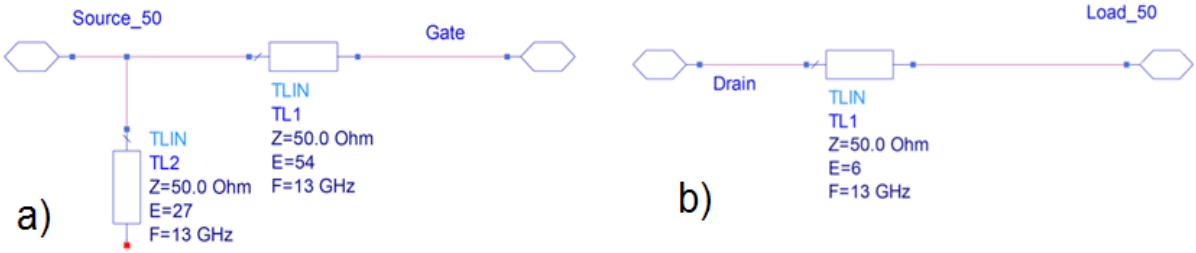

Fig. 6. Matching network for a) source. b) load.

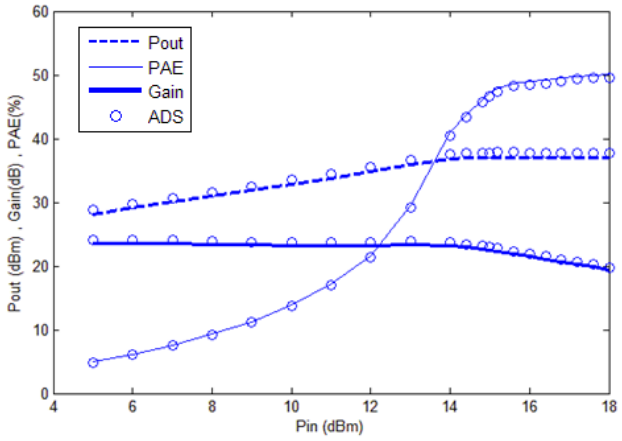

Fig. 7. Single transistor PA design results.

3- 1- 2- Step 2: Designing bias points, Z_s and Z_l with considering PA's linearity

Non-linear HB analysis core presented in section 2-3 , can be done for different bias points, Z_s , Z_l and input powers. This is done for V_{ds} between 20 to 35 V (1 V steps), V_{gs} between -3 to 0 V (0.1 V steps), 20 points in a disk around 5 + j50 with radius of 0.2 in Smith chart for Z_s, 200 points in a disk around 50 + j20 with radius of 0.5 in Smith chart and input power from 10 dBm to 24 dBm (1 dB intervals).

This alone can be time-consuming process, but with storing results after each analysis and use them as next successive analysis start point, this became faster and took about 30 hours to respond, because each change in states are so small that results are close in two successive analysis.

Bias point, Z_s and Z_l choosing criterion were output power over 37 dBm and PAE more than 40 % at 1 dB gain compression point. 1 dB gain compression point can be calculated, because of input power sweep for each condition. $Z_l = 50 + j18$, $Z_s = 5 + j49$, $V_{ds} = 30$ V and $V_{gs} = -1.1$ V were found to be suitable. Source/load impedances at other harmonic was considered zero in this analysis.

3- 1- 3- Step 3: Full search, considering linearity, bandwidth and other harmonics

Z_l and Z_s impedances at other harmonics are specified with matching networks. 8 two-element transmission line matching network were designed to generate Z_l and Z_s at fundamental frequency. Analysis done for each combination of these networks (64 pair) and matching network parameters was swept from 90% to 110% (with 5% intervals) of designed value, input power swept from 10 dBm to 24 dBm (with 1 dB steps), V_{ds} from 27 to 33 V (0.5 V steps), V_{gs} between -1 to -1.3 V (0.05 V steps). Analysis done at different frequencies, 12.4 GHz, 13 GHz and 13.6 GHz. Best performance was seen at $V_{ds} = 30$ V, $V_{gs} = -1.05$ V and matching networks which shown in Fig. 6.

Resulting output power, power gain, and PAE is shown in Fig. 7. Thin line shows analyzed PAE, thick line shows analyzed power gain, dashed line shows analyzed output power and circles shows Agilent ADS simulation results.

Resultant output power was 37.49 dBm, PAE of 47.8% and 22.9 dB power gain at 1 dB gain compression.

3- 2- Power combining

For increasing output power, a number of single transistor amplifiers were designed to work together and their output powers are combined. Power combining can be performed at three levels. First level is performed at chip or die layer, which is increasing active elements to boost current and output power. Second level is done at circuit level, by power combiner circuits and couplers like Wilkinson, branch-line and Lange couplers. Third level can preformed at space, with some aligned radiative elements. The first and second method can be done in an amplifier design, the third one is done out side of amplifiers.

Power combining in chip is done here, by integrating 12 arms of 125 μ m periphery device in a chip. Power combining

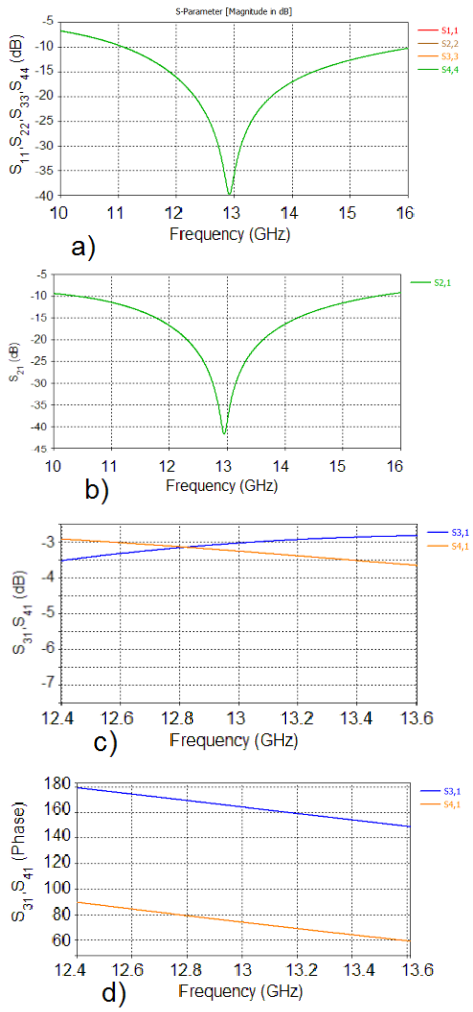

Fig. 8. Designed branch-line coupler a) Matching. b) Isolation. c) Amplitude imbalancy.. d) Phase response Maximum deviation

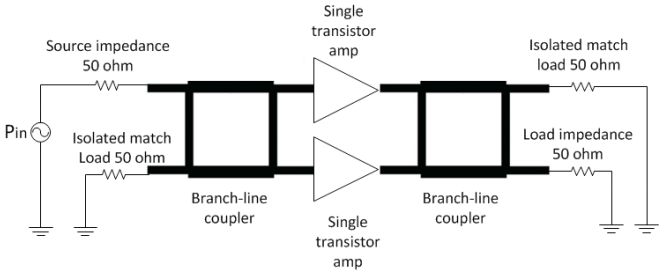

Fig. 9. Designed balanced amplifier.

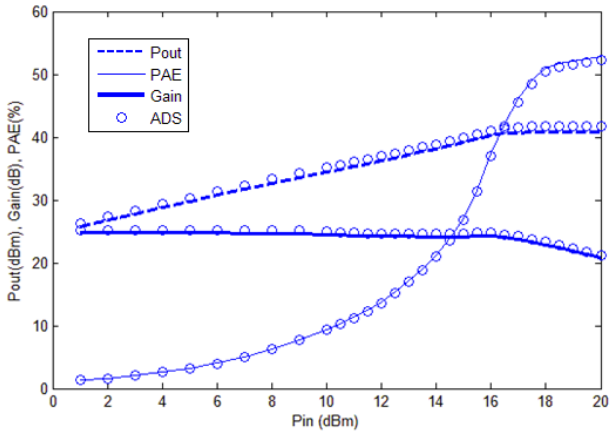

Fig. 10. Balanced amplifier design results.

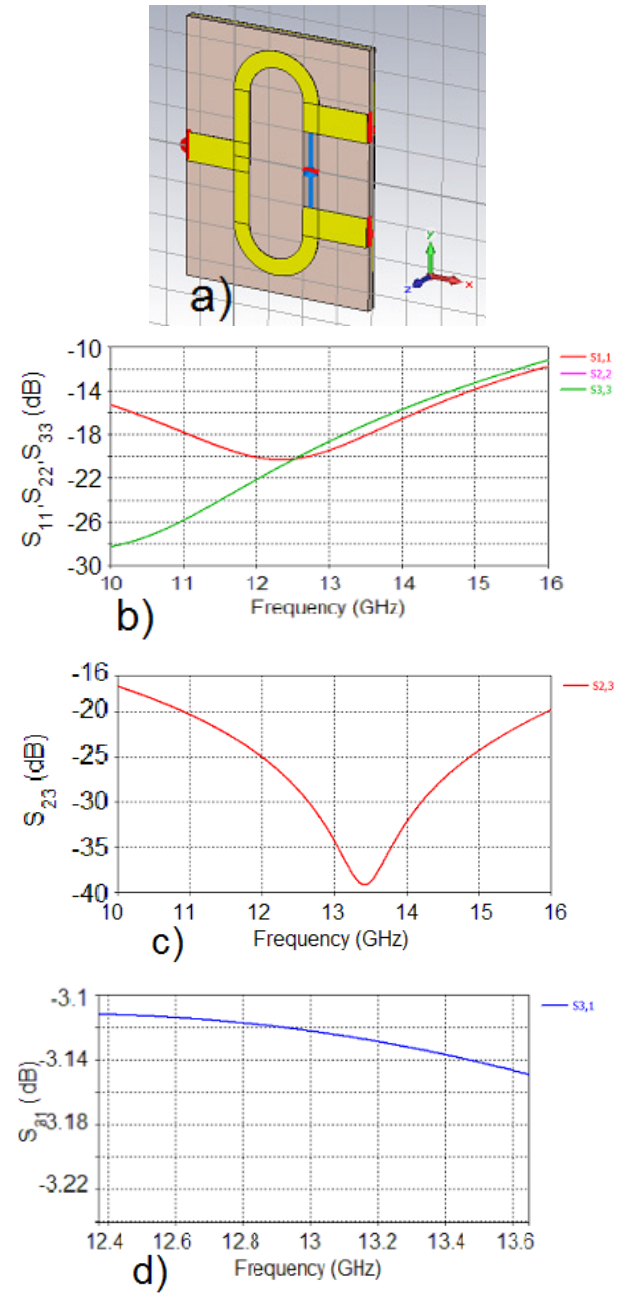

Fig. 11. a) Designed Wilkinson power combiner in CST. b) Matching. c) Isolationd) Loss.. 0.15 dB is maximum loss in output ports.

in circuit level can be done with N-way combiners, which combine N single transistor amplifier outputs together in a single stage, or a three of two way couplers in $\log_2$ N stages. With increasing N, N-way combiners have better performance than tree combiners, like lower loss and wider bandwidth, but it is show in [14], for N$\leq$ 8, tree combiners have better performance. For achieving 40 W of output power, 8 single transistor amplifier designed above is needed to combine, so tree combiners are selected. Each combiner has a determined loss from radiation, conductive loss, dielectric loss, dielectric loss and unmatched connections. Phase and amplitude imbalance can also reduce combiner efficiency[15]. If L was total loss for each two way coupler, which made a combiner tree with K layer, total combiner efficiency is [16]

$$\eta_T = L^{-K}(1-\frac{L^{2K}}{G}) \tag{15}$$

with amplifier block gain G. Eq. (15) shows lower loss, lower layers and higher amplifier gain, result higher efficiency.

An effective technique for combining two elements is balanced structure, which may widen amplifier bandwidth to combine bandwidth, improve VSWR, and also combine output powers[17]. This technique needs 90-degree phase shift that is taken form branch-line couplers. After designing balanced amplifier, four balanced amplifiers are combined by a power combiner tree to produce desired output power. Branch-line couplers have flat architecture, suitable for microstripe circuits, and produce 90-degree phase difference at output branches, suitable for balanced amplifier. A branch-line coupler is designed on RT5880 at 13 GHz and simulated using a full wave simulator, namely CST. RT5880 has low loss tangent (0.0009), which would increase efficiency, and low ϵ_r (2.2), which will increase circuit dimensions and microstripe accuracy in fabrication process, and results in better phase balance and better efficiency.

Designed branch-line results are shown in Fig. 8. Designed coupler has 0.15dB loss, 0.4dB amplitude imbalancy and 3° phase imbalancy over desired frequency range, which would be sufficient for this design.form 90 is 3.

Two single transistor amplifiers are connected with two similar branch-line couplers and yield a balanced amplifier as shown in Fig. 9. For analysis, CST S-parameters output file for designed branch-line coupler was added to passive linear part in linear-nonlinear separation of elements in Agilent ADS, and new 12× 12 Y-parameters for linear part was calculated. Harmonic balance analysis, done for structure as shown in Fig. 9, and HB results are shown in Fig. 10. Thin line shows analyzed PAE; thick line shows analyzed power gain, dashed line shows analyzed output power and circles show Agilent ADS simulation results. Maximum output power was 40.63 dBm, PAE was 46.7%, and 23.13 dB power gain was at 1 dB gain compression.

For reaching 40 W, at least four balanced amplifier needs to be combined. Maximum combiner loss due to output power would be

$$\eta_T = L^{-K}(1-\frac{L^{2K}}{G}) \tag{16}$$

$$L_{combiner} = -10\log(\frac{P_{out_{desired}}}{4\times P_{out_{balanced}}}) = 0.63\,dB \tag{17}$$

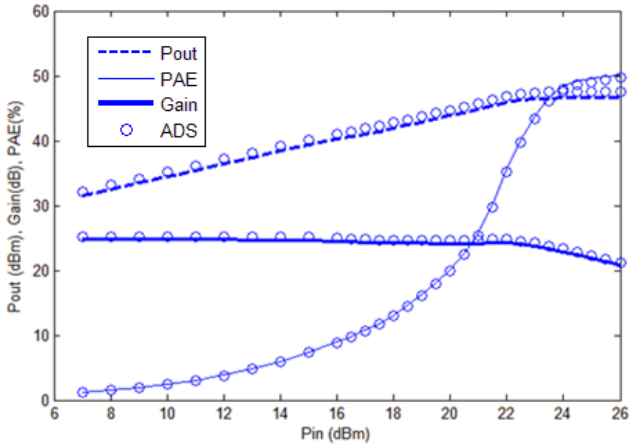

Fig. 12. Total analysis of amplifier gain, PAE and output power, and simulated results in Agilent ADS.

Maximum combiner loss due to PAE is

$$L_{combiner} = -10\log(\eta_{min_{combiner}}) = -10\log(\frac{PAE_{desired}}{PAE_{balanced}}) = 0.67\,dB \qquad (18)$$

which $PAE_{desired} = PAE_{balanced} \times \eta_{combiner}$. Combiner loss have to be under 0.63 dB, i.e. the minimum result of equations (16) and (17).

A Wilkinson power combiner is designed and simulated over RT5880 in CST, and output S-parameters file is used in Agilent ADS to generate power combiner tree and, thus, calculate 42× 42 elements of Y-parameters for this structure. Wilkinson power combiner S-parameters are shown in Fig. 11. As shown in Fig. 11, maximum loss is 0.15 dB, so power combiner tree with two stages is sufficient for producing desired output power and PAE.

With using 42× 42 Y-parameters matrix, total amplifier structure is analyzed. Fig. 12 shows total amplifier results. Thin line shows analyzed PAE, thick line shows analyzed power gain, dashed line shows analyzed output power and circles show Agilent ADS simulation results. Maximum output power was 46.3 dBm, PAE was 43.3% and 21.9 dB power gain at 1 dB gain compression. Fig. 13 a) and b) illustrate I_{ds} for main harmonic and total harmonics, respectively. Fig. 14 a) and b) shows V_{ds} and V_{gs} for transistors.

4- Conclusion

In the presented paper, total designed power amplifier schematics was shown in Fig. 14. Output powers of each

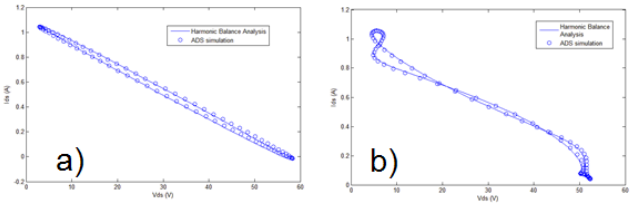

Fig. 13. Load cycle of transistors. a) main harmonic. b) total harmonics.

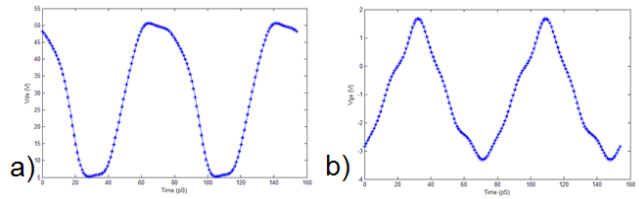

Fig. 14 a) V_{ds} b) V_{gs} of transistors over a two-cycle in time domain.

transistor amplifiers and balanced amplifiers are 37.7 dBm and 40.63 dBm, respectively. Output power of first stage Wilkinson's power combiner reaches at 43.45 dBm and 46.3 dBm at second power combiner stage. With new presented design procedure,a high power (46.3 dBm) and high power added- efficiency (up to 43%) solid state power amplifier at Ku band is designed.

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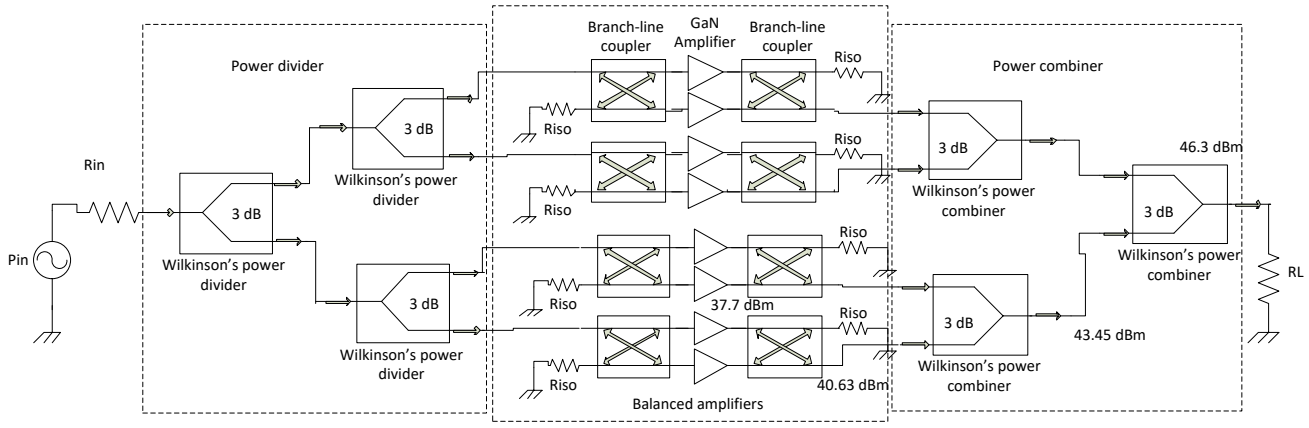

Fig. 15. Total designed power amplifier schematics. Power dividers, balanced amplifiers and power combiners blocks are specified.

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Please cite this article using:

V. Ezzati and A. Abdipour, Non-linear modeling, analysis, design and simulation of a solid state power amplifier based on GaN technology for Ku band microwave application, *AUT J. Model. Simul.*, 50(2) (2018) 195-202.

DOI: 10.22060/miscj.2018.13414.5072