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Single-ended 6T SRAM Cell with Low Power/Energy Consumption and High Stability

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ABSTRACT: In this paper, we propose 6T cell with single-ended characteristics to achieve an improved stability, decrease energy consumption, and decrease leakage power. The cell is compared with strong 10 and 12 transistor structures with good and excellent specifications. However, the above structure is designed to have the best parameters with low size and a minimum number of transistors that reduce the size of the cell. In some parameters, such as the write noise margin, the structure has the best merits in comparison with other structures, even higher than the structures of 12 and 10 transistors. The write operation is enhanced by cutting the pull-down path to the storage node to be written as "1"; the read operation is performed without cutting the pull-down path. At VDD=0.4V, the static power, read margin, write margin, read energy, and write energy of the proposed structure are superior by 33%, 50%, 215%, 9%, and 5%, respectively, in contrast to the traditional 6T. The Electrical Quality Metric (EQM) parameter has been improved about ten times compared with the standard 6T structure, showing that the value of the new structure has been introduced. A Monte Carlo simulation of 5,000 read and write yields in the 32nm technology revealed that our cell has a 2x and 3.4x higher yield than the typical 6T cell. Consequently, the proposed 6T cell is an appropriate option for applications requiring low energy and high robustness.

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1- Introduction

A Static Random Access Memory cell (SRAM) is the primary component of any System on Chips (SoCs). It constitutes a disproportionate share of the overall power budget [1, 2]. Various low-power applications have become increasingly prevalent in recent years, including biomedical devices, wireless sensor networks, the Internet of Things, and the handheld devices. Therefore, managing the power of memory cells has become a crucial matter in SoCs [3]. The cells should also have a minimum number of transistors to enhance density. However, the smaller transistors lead to an increase in process variability. Gate oxide thickness channel doping and channel length variations are process variability exacerbated by scaling. As a result, the chance of malfunctioning of the memory cell increases, lowering the yield [4]. Due to short-channel effects, such as DIBL, scaling also increases leakage exponentially. Therefore, idle SRAM blocks consume more power due to the scaling [5]. A decrease in supply voltage to near-threshold voltage can decline power consumption in memory cells [6-8]. Dynamic power decreases quadratically when the supply voltage is lowered, while leakage power decreases exponentially [9, 10]. The reduction of supply voltage decreases the drivability and noise margin of the memory cell, resulting in a degradation of speed and robustness [11]. In conventional 6T SRAM cells (Fig1 .(a)), at low power supply voltages, the static margins are insufficient due to the intrinsic conflicts in the write and read process. Moreover, transistor threshold voltages influence the performance of the cell [12]. Therefore, there will be a decrease in yield as well as sensitivity to process variation. In order to achieve greater stability in the face of process variability, new structures have been proposed.

In [13], the designers used a Schmitt-trigger inverter to create improved hold stability in their SRAM cell (designated the structure ST-1, Fig. 1(b)). Compared to the 6T cell, this structure possesses a more Read Static Noise Margin gin (RSNM). Despite this, it can still suffer from low RSNM and Write Static Noise Margin (WSNM) at lower supply voltages due to the read disturbance caused by Bitline voltages and a strong back-to-back inverters feedback. In the ST-1 structure, the energy consumption of read and write is higher than the 6T structure, and ten transistors are used per cell, increasing the cell area. Process variation effects can exacerbate the ST-1 characteristics similar to the 6T structure without significant improvements.

The WRE8T scheme has been proposed for overcoming low WSNM (Fig. 1(c)). By weakening the left inverter in the write state, WSNM is increased [14]. However, HSNM and

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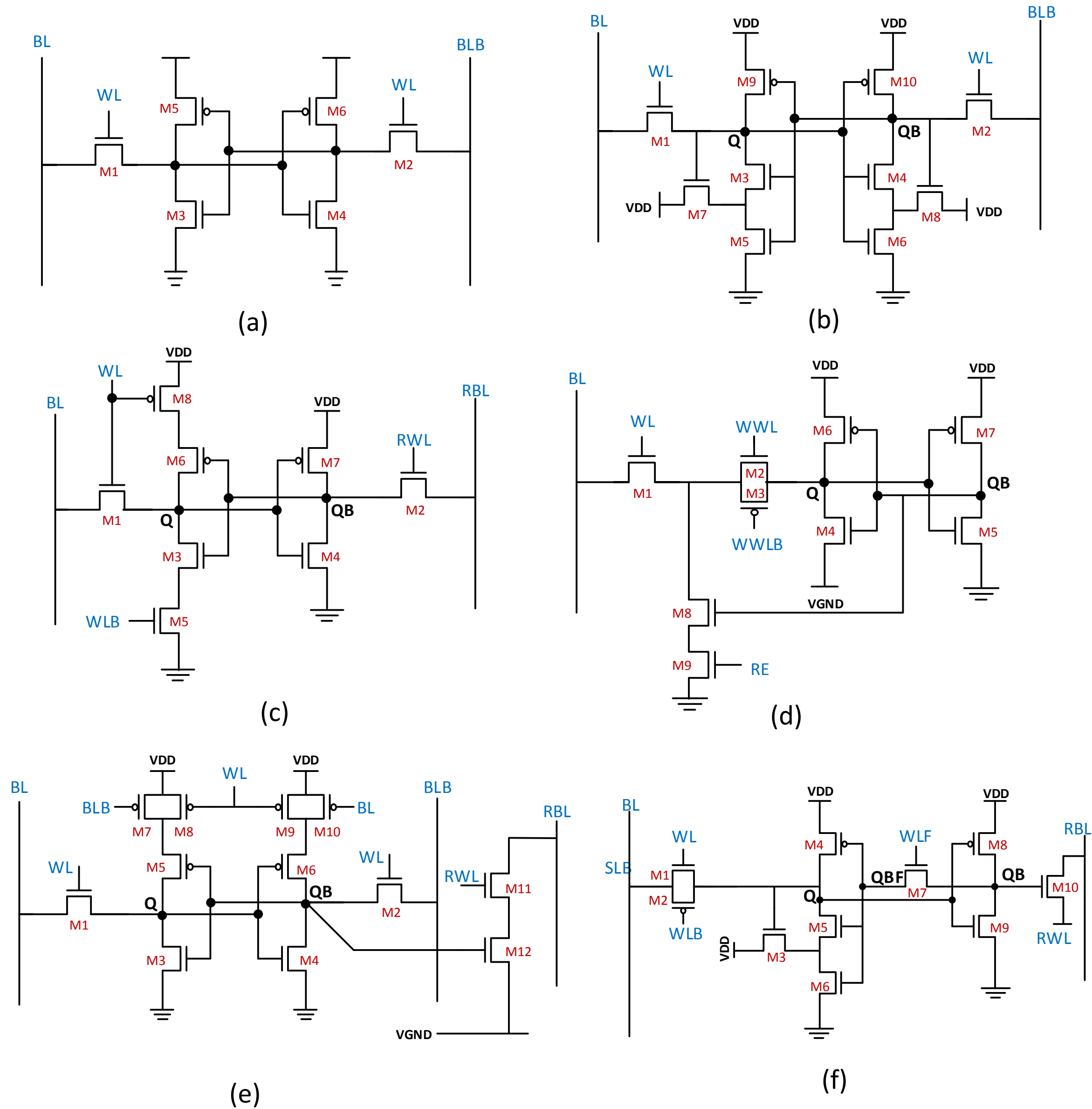


Fig. 1. The schematic depicting different memory cells (a) 6T (b) ST-1 [13] (c) WRE8T [14] (d) SB9T [15] (e) 12T [16] (f) 10T cell [17]

RSNM are still insufficient at low supply voltages, and even RSNM is inferior to the 6T structure. An SB9T structure has been proposed to alleviate leakage power [15] (Fig. 1(d)). The structure suffers from low ‘0’ WSNM, and its read and write speed is also less than other structures due to the single-ended structure. Additionally, this structure has much more write and read energy compared to other structures. The 12T structure [16] (Fig. 1(e)) and 10T [17] (Fig. 1(f)) have been proposed to improve WSNM. These structures improve RSNM, read and write time is also suitable, but the structures are 12T and 10T and have enormous dimensions. Furthermore, they consume high amounts of power to read and write, and leak more than other structures.

This work proposes a 6T single-ended SRAM that exhibits outstanding low-power and stable characteristics. As mentioned earlier, read and write noise margins are crucial parameters of an SRAM cell. Resistance to process variations, reduction of leakage power, and reduction of write and read energy are also the primary characteristics of SRAM memory cells. Although the proposed SRAM is single-ended, and is designed to have all the primary features of a cell. The rest of the paper is arranged as follows. The proposed cell structure and its function are elaborated in Section 2. Section 3 compares several proposed cell performance and stability metrics with those of other SRAM cells. In Section 4, the paper is summarized and concluded.

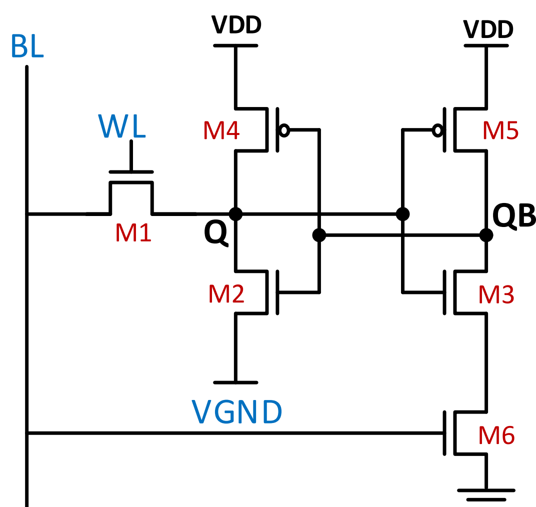


Fig. 2. Schematic for the proposed 6T SRAM cell

Table 1. List of the voltages used to control the proposed 6T cell.

signals	Hold	Read	Write '0'	Write '1'
WL	GND	V_{DD}	V_{DD}	V_{DD}
BL	V_{DD}	Pre-charge	GND	V_{DD}
VGND	GND	GND	V_{DD}	V_{DD}

2- Proposed SRAM Cell

A number of previously introduced structures have relatively low read and write noise margins at low supply voltages. However, some use more transistors to expand the write and read noise margin, thereby increase the area. Our goal is to achieve the best parameters and specifications for an SRAM cell with the minimum number of transistors and dimensions. Fig. 2 illustrates the proposed 6T cell. A single-ended write operation is accomplished using transistors M1, M2, and M6, and a single-ended read operation is accomplished using transistors M1 and M2. The single-ended operations reduce the effective capacitances switching during the operations and consequently decrease the dynamic power consumption. Furthermore, eliminating one access transistor compared to differential structures decreases the leakage paths, thereby reduces the static power. In addition, we have added a transistor (M6) to enhance the write Static Noise Margin. The source of M2 is connected to the 'VGND' control line, facilitating the writing of '1'. The Bitline (BL) and the Wordline (WL) are for the read, and the Bitline (BL) and Wordline (WL) and VGND are utilized for the write operation. The following subsections discuss our proposed design of the cell and its working mechanism in different states. The control signal values of the design are shown in Table 1.

2- 1- Write State

To trigger the write operation, first BL is set to the target data, then by asserting the WL and VGND signal, the write operation is completed. When initially Q = '0' and one wants to write '1' in this node, all BL, WL, and VGND will be set to V_{DD}, turning on M1 and M2 charging Q node from BL and VGND without any conflict. When the voltage at the node Q surpasses the right-side inverter threshold voltage, which

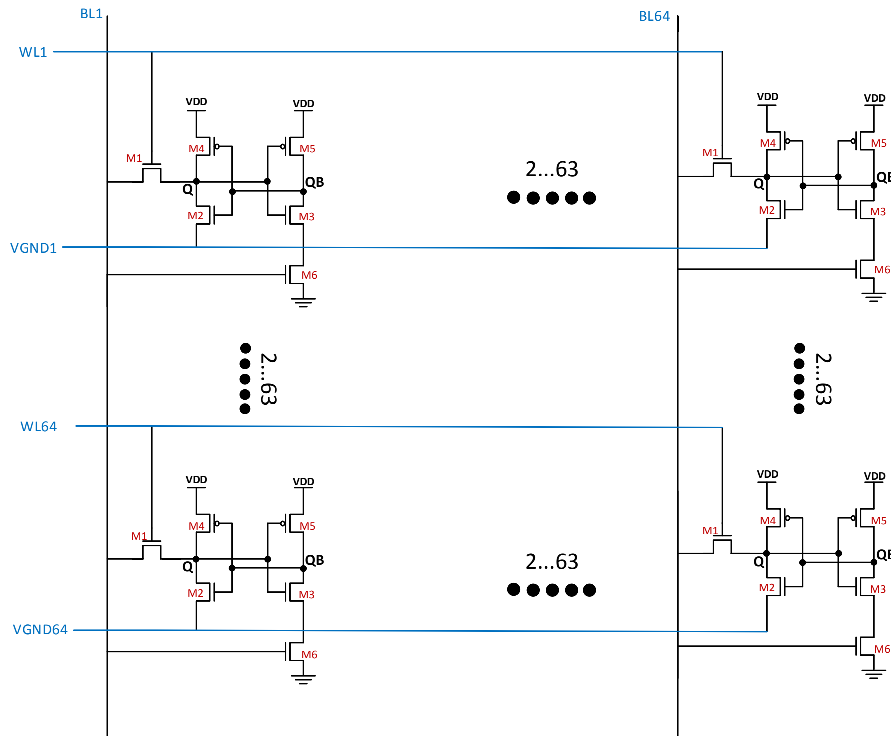


Fig. 3. The proposed 6T cell array.

comprises M3, M5, and M6, the positive feedback completes the write operation. If at first, Q = '1' and one wants to write '0' on it. The grounded BL shuts off M6, disconnecting the pull-down path to the QB node. The Q node is discharged through M1 (which is nMOS and good in passing '0'), and QB is charged by turning on M5 without any intrusive pull-down. After settling into the hold state and grounding WL and VGND, the Q node becomes solid '0'.

2- 2- Read State

In order to start a read operation, WL is set to $V_{DD,}$ and BL must be pre-charged to V_{DD}, as shown in Table 1. When Q = '0' and QB = '1', M1 and M2 turn on discharging BL, and the sense amplifiers accomplished the read; when QB = '0', BL stays pre-charged at V_{DD}. Since M2 is bigger than M1, the charge sharing between the data node Q and the Bitline is small. In this structure, the size of the transistors is considered in such a way that parameters RSNM and HSNM are equal (similar to separate structures 12T and SB9T).

2- 3- Hold State

In the hold state, leakage power is of primary importance. In the hold, the BL voltages are at V_{DD}. All voltages of WL and VGND are GND to decouple Q and QB nodes from the Bitlines and preserve data on Q and QB nodes.

3- Results and Discussion

This section compares the proposed memory cell with other related SRAM cells. A comparison of conventional 6T, ST-1 [13], single-ended WRE8T [14], SB9T [15], 12T [16], and 10T [17] cells have been made (Fig. 1). We conducted HSPICE simulations [15] at the 32 nm technology for all SRAM structures to create a uniform comparison platform. Simulations of time and EDP were based on 64 array structures (Fig. 3). Capacitances of interconnects were assumed to be 0.16 fF [17]. The transistor widths of the structures are listed in Table 2. All proposed cell transistors except M1, M3, and M4 have a minimum size to facilitate the compact design and reduce power consumption. The transistor sizes for the other cells have been adopted from the original proposal. We ran on 5,000 sample Monte Carlo simulations to analyze process variability effects. Similar to [18], it was assumed that the channel length, channel width, channel doping, gate oxide thickness, and threshold voltage distributions would be Gaussian with a 10% variation (3σ).

3- 1- Read Stability

RSNM is a prominent metric for evaluating read stability. RSNM is determined by the length of the square enclosed in the smaller lobe of the read butterfly curve [19-21]. Fig. 4(a) shows the high RSNM compared to

Table 2. Transistor sizing of different cells.

Cell	Transistor	W/L Ratio ($\lambda = 0.016\ \mu m$)
6T	M1, M2	$7\lambda/2\lambda$
	M3, M4	$9\lambda/2\lambda$
	M5, M6	$4\lambda/2\lambda$
SB9T	M1, M2, M3	$8\lambda/2\lambda$
	M4, M5, M6, M7, M8, M9	$4\lambda/2\lambda$
ST-1	M1, M2, M3, M4, M5 M6, M7, M8, M9, M10	$4\lambda/2\lambda$
WRE8T	M1, M2, M3, M4, M5 M6, M7, M8	$4\lambda/2\lambda$
12T	M1, M2, M3, M4, M5, M6, M7, M8, M9, M10, M11, M12	$4\lambda/2\lambda$
Proposed 6T	M1	$4\lambda/2\lambda$
	M2	$5\lambda/2\lambda$
	M3, M4	$4\lambda/4\lambda$
	M5, M6	$4\lambda/2\lambda$
10T	M3, M5, M6, M7, M9, M10	$4\lambda/2\lambda$
	M1	$8\lambda/2\lambda$
	M2	$6\lambda/2\lambda$
	M4	$4\lambda/4\lambda$
	M8	$5\lambda/2\lambda$

6T, WRE8T, and ST-1 structures. The SB9T, 10T, and 12T structures have a high RSNM due to an isolated circuit for reading, which has increased the cell size. As a result, the proposed structure has a higher RSNM than its peer structures at different supply voltages. The read stability for structures that use a separate path for reading (such as SB9T, 10T, and 12T) from Q and QB nodes are high. In Fig. 4(b), read yields are shown for different SRAM cells in conditions of process variation. As shown, our proposed structure achieves the read yields of more than 15σ for all supply voltages. On the other hand, while there is a Bitline coupling to storage nodes throughout a read (such as WRE8T and 6T) in the proposed structure, there is a high read yield meeting the minimum six-sigma requirement of large SRAM arrays [6, 22].

3- 2- Write Ability

There are several approaches for evaluating WSNM. One of those is the maximum change in voltage on the write Bitline till Q becomes equal to QB, producing a successful write [23, 24]. Fig. 5(a) shows that the proposed cell has the highest WSNM '0' compared to other understudy cells at different supply voltages. The proposed structure also has the highest WSNM '1' compared to the ST-1 and 6T structures (Fig. 5 (b)).

A disadvantage of single-ended cells is their inferior write '1' performance due to using n-channel access transistors.

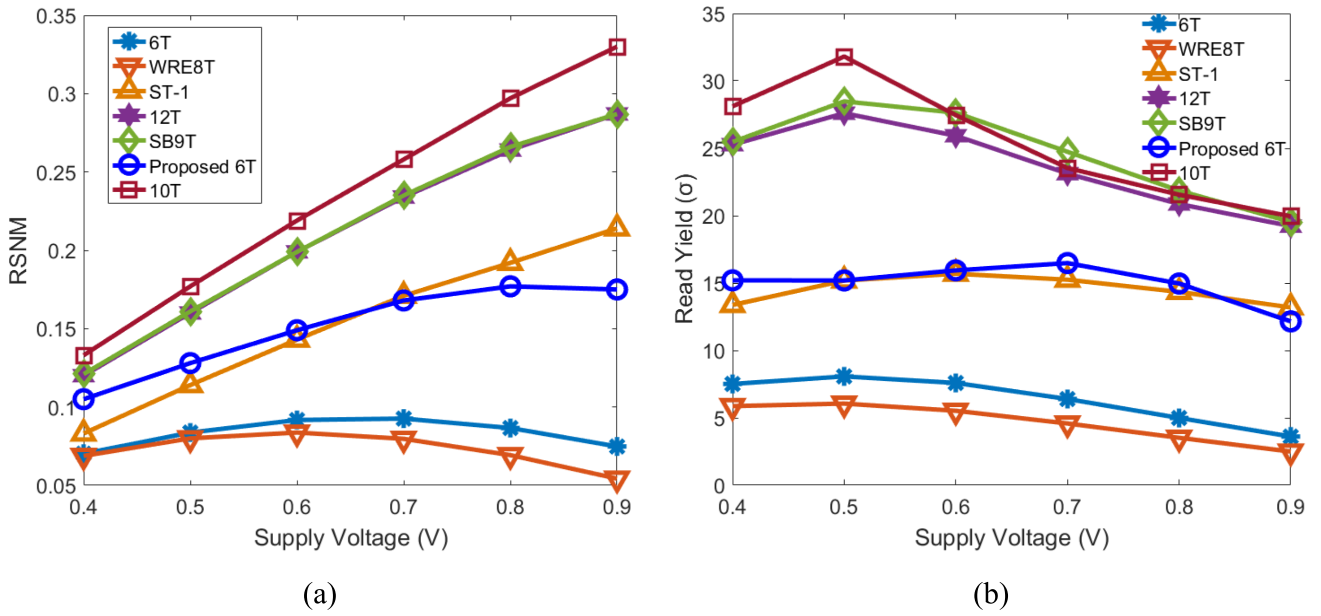


Fig. 4. (a) RSNM and (b) read yield for various supply voltages.

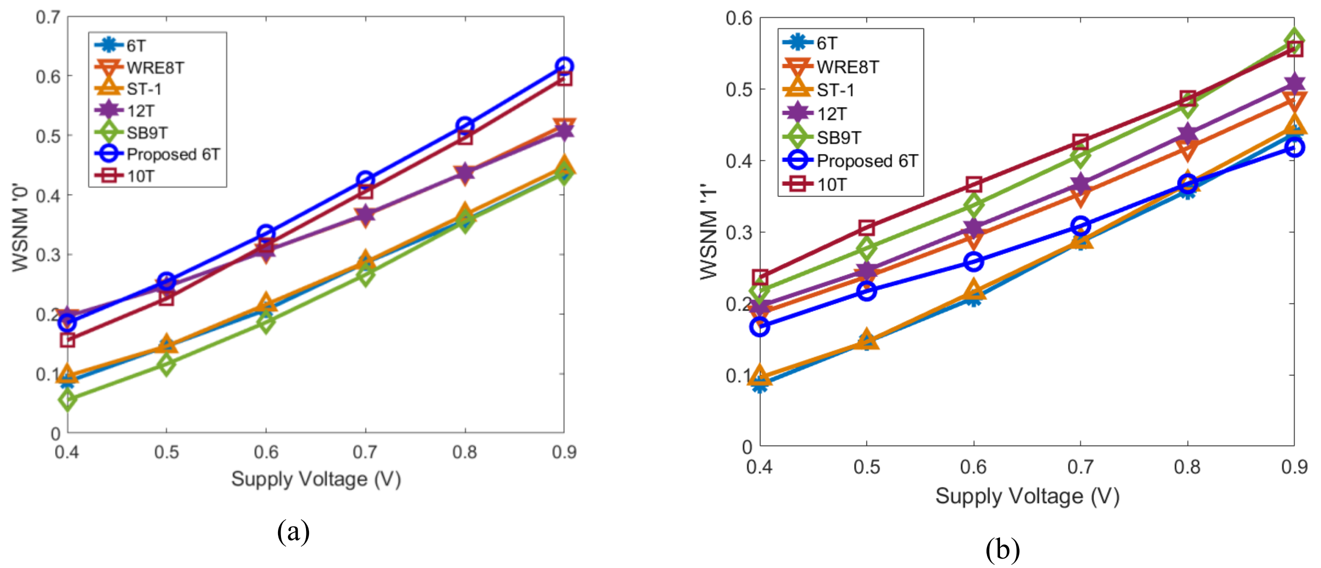


Fig. 5. Comparison of (a) WSNM' 0' and (b) WSNM' 1' for different supply voltages.

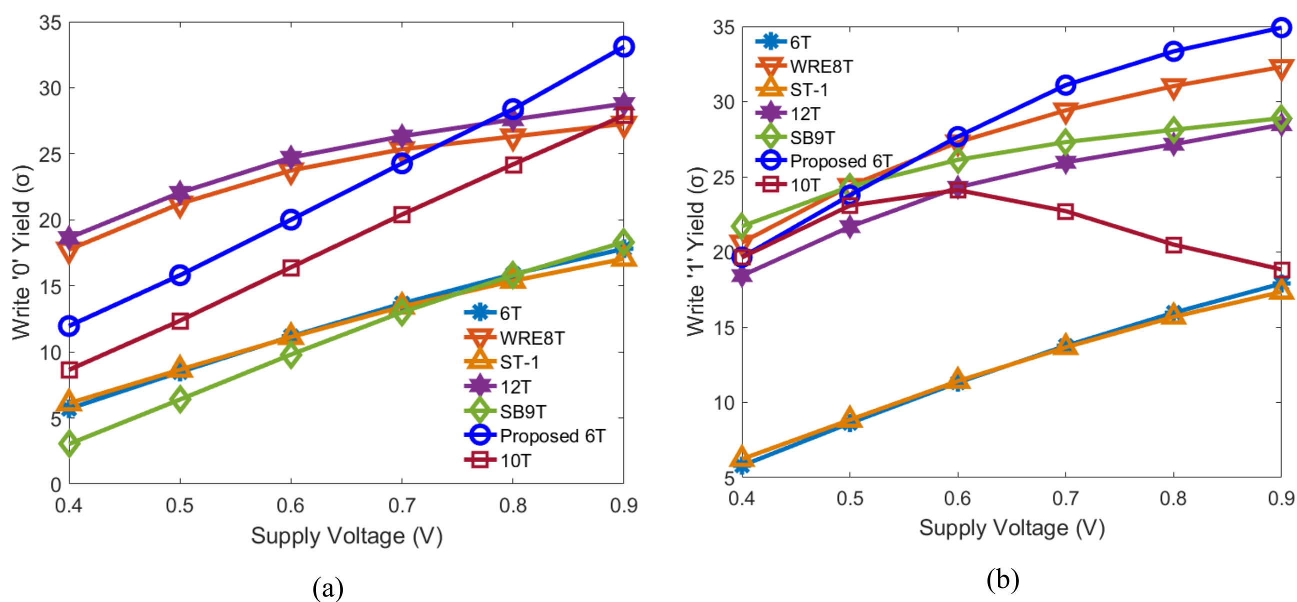


Fig. 6. (a) Write '0' yield and (b) write '1' yield versus supply voltage for different SRAM cells.

As a solution to this problem in the proposed structure, the pull-down path is eliminated for node Q by setting VGND to VDD. For the write '0' of the proposed SRAM, the pull-down path for node QB is cut by turning off M6, leading to a relaxed and robust operation. The write ability of 6T and ST-1 and SB9T (write '0') is low due to a strong back-to-back inverters feedback. The proposed cell has a higher write yield than 6T, ST-1, 10T, and SB9T and is in the range of 12T and WRE8T (Fig. 6). As illustrated, the write yields of the proposed structure are more than 12σ, exceeding the minimum requirement of six sigma for all supply voltages.

3- 3- Hold Stability

As HSNM, the butterfly curve method is also employed to assess hold stability. HSNM indicates the amount of storage node noise voltage that the cell can tolerate when the data remains unaffected in the hold state [25]. Fig. 7(a) shows that the proposed structure has the lowest HSNM value. Although the separate route is not used for read operations in the proposed structure, the proposed structure is adjusted so that the value HSNM and RSNM are equal. To increase HSNM, the transistor lengths M2 and M5 can increase, but this method reduces RSNM. As shown in Fig. 7(a), HSNM is lower than other structures, but the obtained HSNM is not a small amount and is acceptable. The HSNM of the symmetric ST-1 is the highest amount since it uses Schmitt-trigger inverters. The hold yields are shown in Fig. 7(b). The other cells have a high hold yield (more than 15σ), except the proposed structure, because during the hold state, the Bitlines are isolated from the storage nodes. In the proposed structure, we have a high hold yield (more than 15σ) at voltages of 0.5V and 0.6V, and in all supply voltages, it has a hold yield of more than 10σ.

3- 4- Read/Write time

Fig. 8 shows the read access time for different cells. As seen, the proposed cell has the fastest read among the related cells, except for the 6T and 10T SRAM cells with a shorter read time. Fig. 9 illustrates the write time '0' and '1' for different structures. While the proposed cell write time is more than differential cells, this slower write is compensated at high supply voltages and approaching differential structures.

3- 5- Dynamic Energy

Reading and writing are components of dynamic energy consumption. The proposed cell consumes the lowest read energy, as illustrated in Fig. 10(a). The read circuits for structures 6T and ST-1 are almost identical to the proposed structures. However, the proposed structure has less read energy than the ST-1 and 6T due to its higher control signals and larger cell dimensions (length and width). It is worth mentioning that the minimum size for the access transistors is not considered in the 6T cell. Additionally, the gate capacitances of two access transistors can affect the control signal WL. As an alternative, the gate capacitance of a transistor in the proposed structure affects the control signal WL, and the transistor has a minimum size. As a consequence, the proposed structure has a read energy of less than 6T. In structure 12T, SB9T, 10T, and WRE8T, a large cell area (length and width) increases the capacitance and read energy.

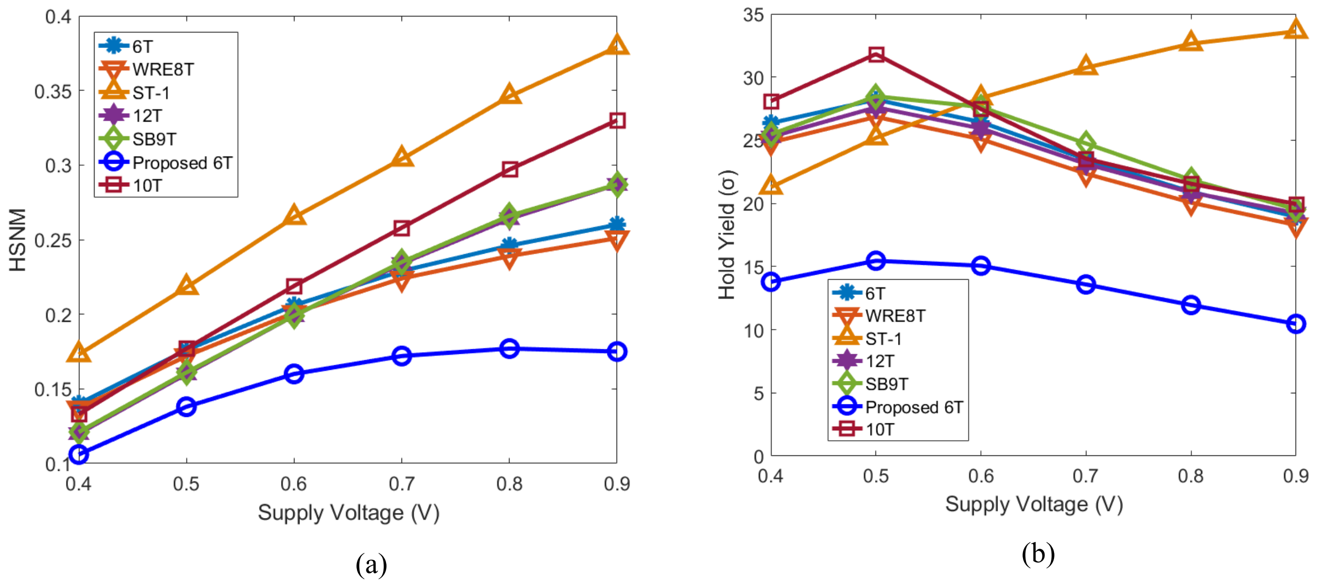


Fig. 7. (a) HSNM and (b) hold yield versus supply voltages for different SRAM cells.

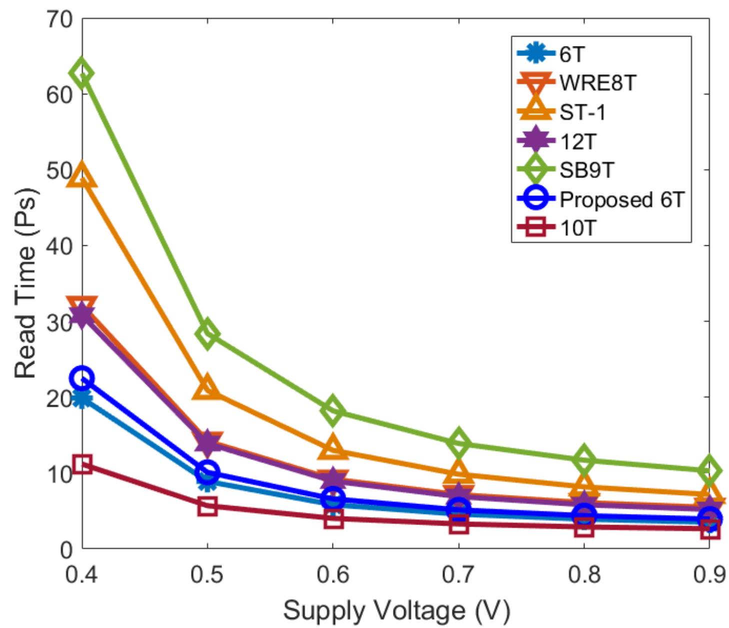


Fig. 8. Comparison of read times for different supply voltages.

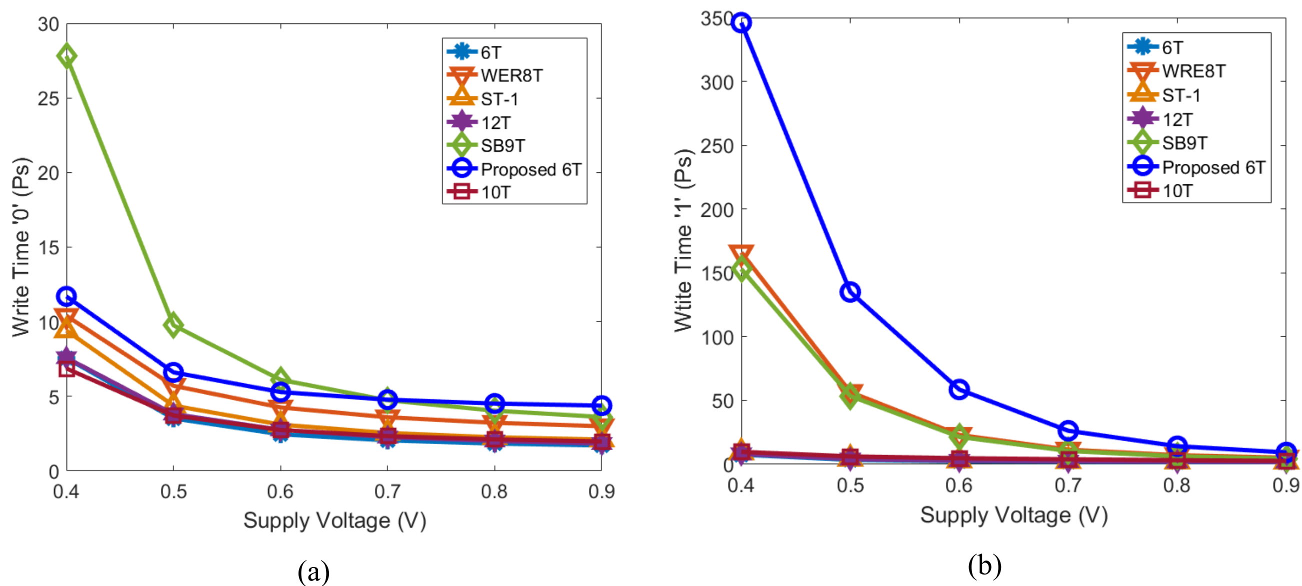


Fig. 9. (a) write time '0' and (b) write time '1' versus supply voltage.

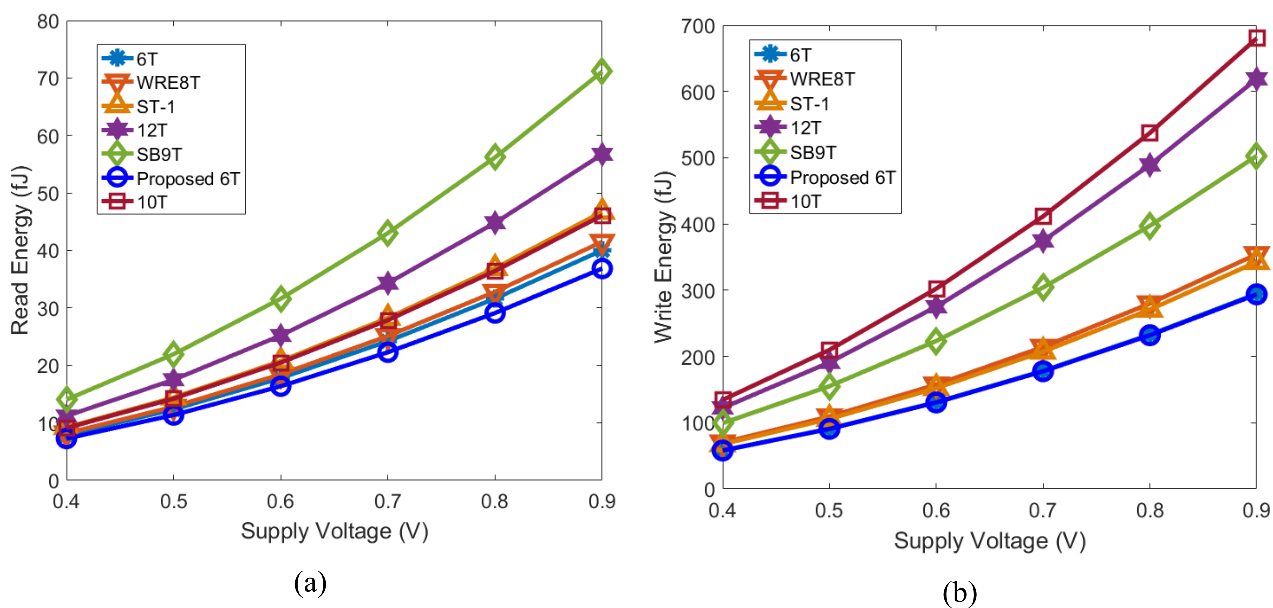


Fig. 10. (a) Read energy and (b) write energy consumption versus supply voltage.

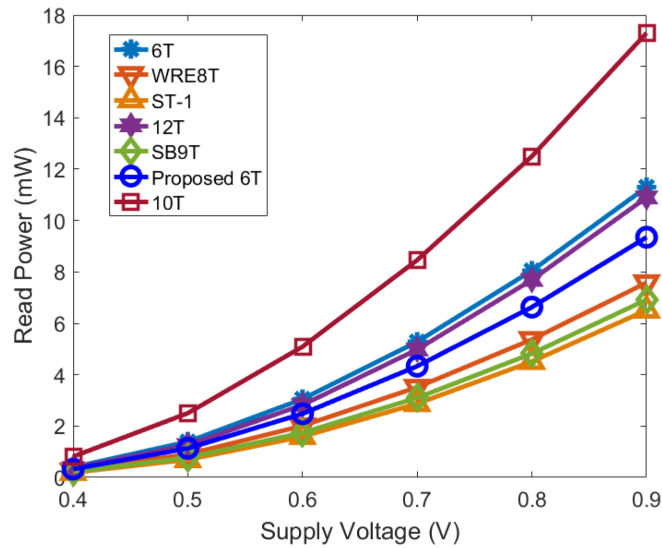


Fig. 11. Read power consumption versus supply voltage.

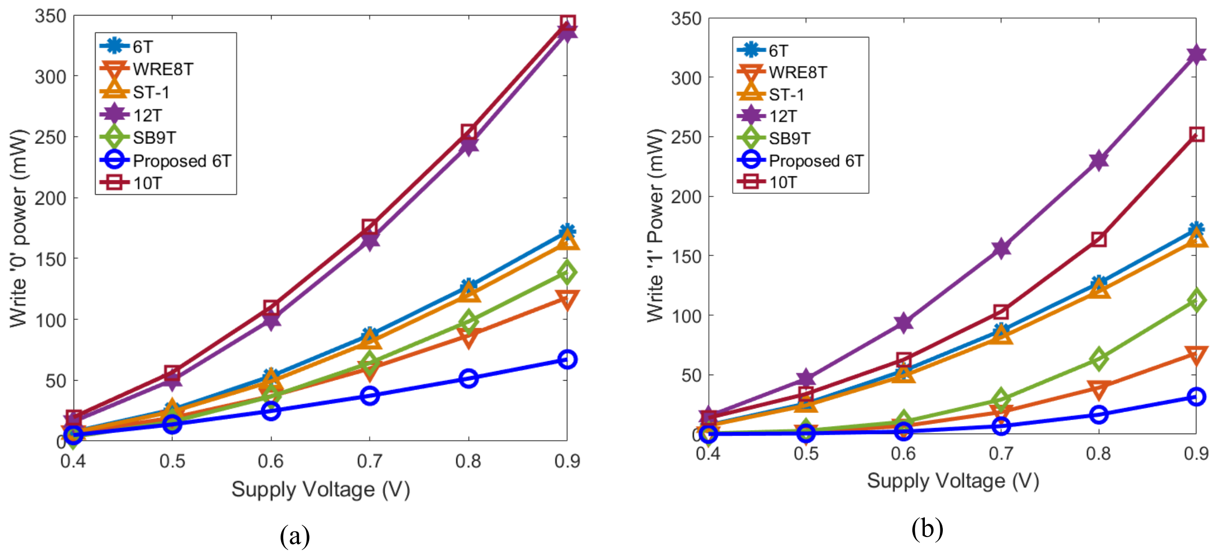


Fig. 12. (a) write power '0' and (b) write power '1' consumption versus supply voltage.

In the same way, as explained for read energy, the number of control signals, cell area (cell length and width), and the transistor sizes all contribute to increased dynamic energy consumption in the write state. The proposed cell has lower write energy than other cells (Fig. 10(b)).

3- 6- Dynamic Power

Dynamic power comprises write and read parts. According to Fig. 11, the proposed cell has lower read power compared with 12T, 10T, and 6T cells, but slightly higher than SB9T, WRE8T, and ST-1 cells for all supply voltages. SB9T, WRE8T, and ST-1 have low read power due to slow read operations. The proposed SRAM cell has a lower write power because of the low write energy as compared to other comparable cells (Fig. 12).

3- 7- Static Power

The leakage currents consist of a subthreshold (Isub) and a gate current (Ig). In the technology, the high-k gate oxide is used so the gate leakage is decreased, and the subthreshold

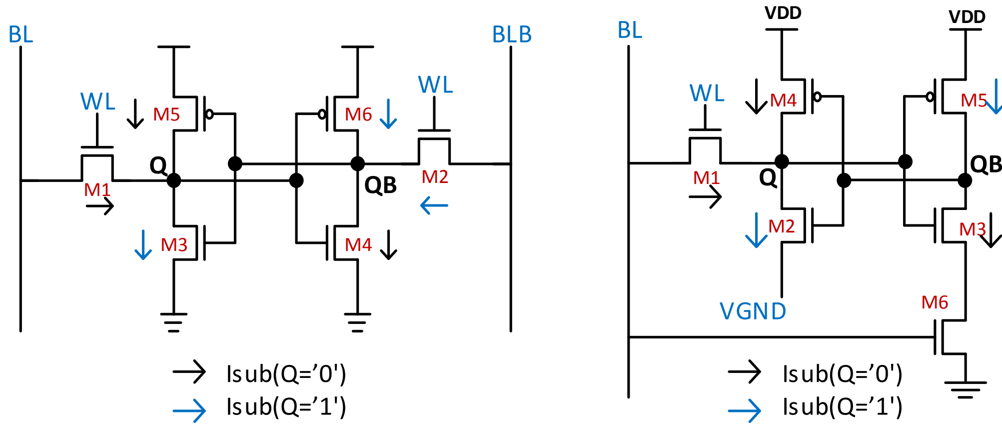


Fig. 13. The leakage current components for (a) the conventional 6T and (b) the proposed cell.

current comprises a noticeable share in total leakage current. When transistors are sized smaller, sub-threshold leakage current increases, causing a higher static power consumption [26]. Figure 13 shows transistors with subthreshold leakage in the 6T cell and the proposed 6T cell. When Q = '0', the leakage currents of the cells are:

$$I_{\text{sub6T}} = I_{\text{sub M1}} + I_{\text{sub M5}} + I_{\text{sub M4}} \tag{1}$$

$$I_{\text{sub Proposed6T}} = I_{\text{sub M1}} + I_{\text{sub M3}} + I_{\text{sub M4}} \tag{2}$$

$$I_{\text{sub6T}} = I_{\text{sub M2}} + I_{\text{sub M3}} + I_{\text{sub M6}} \tag{3}$$

$$I_{\text{sub Proposed6T}} = I_{\text{sub M2}} + I_{\text{sub M5}} \tag{4}$$

If Q = '1', the leakage current calculations are:

As shown in Fig. 14, when Q = '0', the static power of the proposed structure is lower than all structures, and when Q = '1', the leakage power of the proposed cell is more than other cells compared. However, the average static for the proposed design is less than structures WRE8T, ST-1, 12T, 10T, and 6T.

3- 8- Half-select Issue

We assume the entire row is written in the proposed structure as [27]. If this is not the case, the half-select issue can be resolved with a write-back circuit [28]. According to Figure15(a), there may be a problem with the column half-select cell. The issue was investigated through Monte Carlo simulations, using 5,000 samples. A column half-select signal during a write operation at 0.4 V is shown in figure 15(b). In this simulation, the WL and VGND assentation time is about 3x the required time for a write operation. We can see that the amount of change for the QB node is tiny, and the stored values of the Q and QB nodes of the half-select cell are not affected. Therefore, the proposed 6T cell is resistant to half-select issue. It can employ the bit interleaving and Error Correction Coding (ECC) methods that can be utilized to alleviate soft-errors generated by severe space radiations [3, 8, 18, 20, 21].

3- 9- Area Comparison

Fig. 16 shows the layout [22] of cells drawn using L-edit (Tanner EDA). Table3 lists the dimensions and different SRAM cell areas, where λ is 1/2 of L_{min}. The proposed cell has a 1.125x area overhead compared to a 6T cell. The structure 6T has the same transistor numbers as the proposed cell; however, the dimensions of some transistors of the proposed 6T are larger than the minimum size, which increases its area.

3- 10- Electrical Quality Metric

As shown in Table 4, the proposed design outperforms the 6T cells with respect to RSNM, WSNM, static power dissipation, and dynamic power dissipation at V_{DD} = 0.4 V. In addition to the conventional 6T, the proposed cell has the best read performance and compact area. The proposed cell features the lowest static and dynamic power consumption (an increasingly important issue) among the compared cells.

SRAM cells commonly trade off various performance metrics. Thus, to fully measure the performance of an SRAM, we use an Electrical Quality Metric c (EQM) [29] to assess the inclusive cell quality. EQM is:

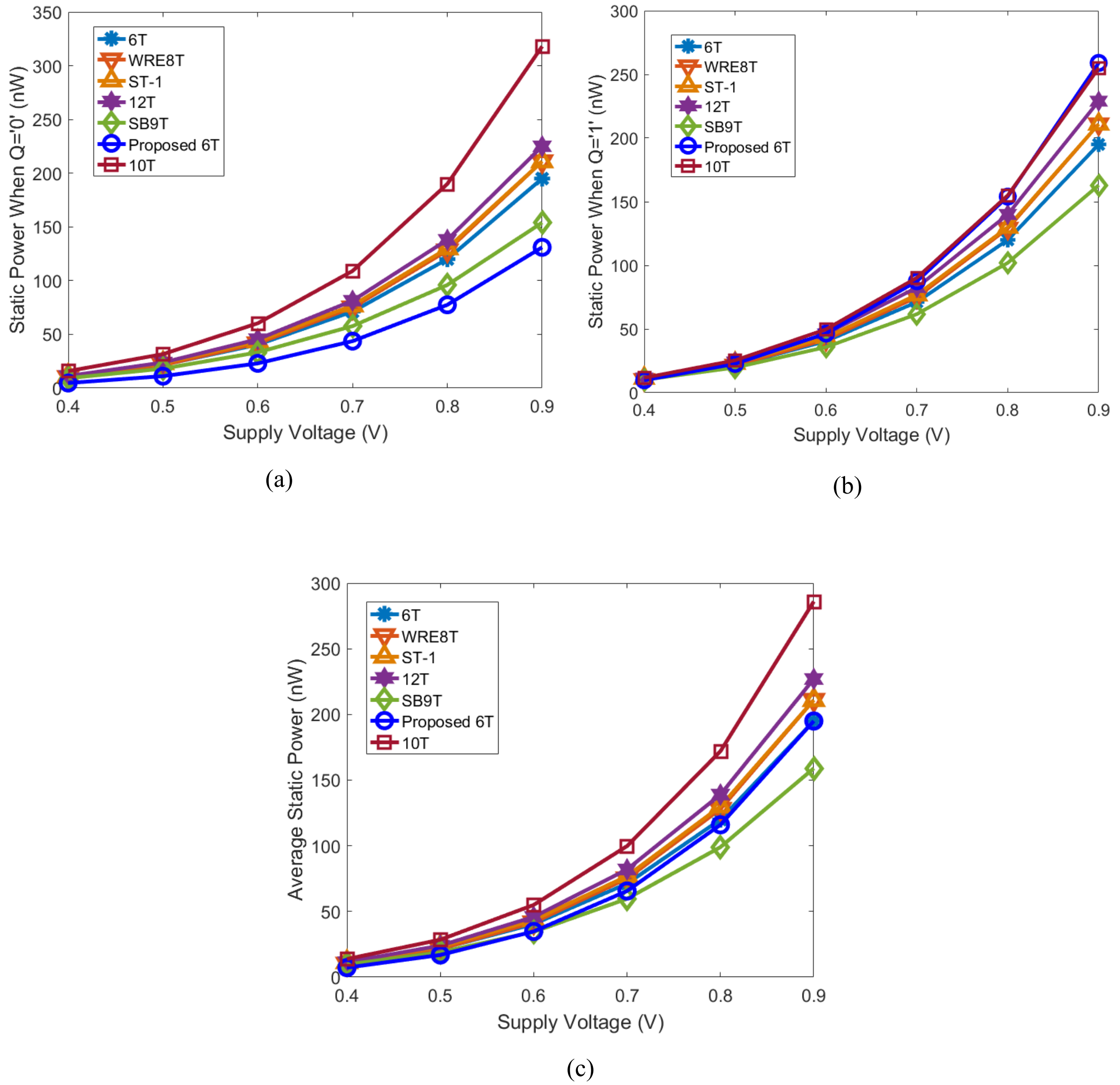
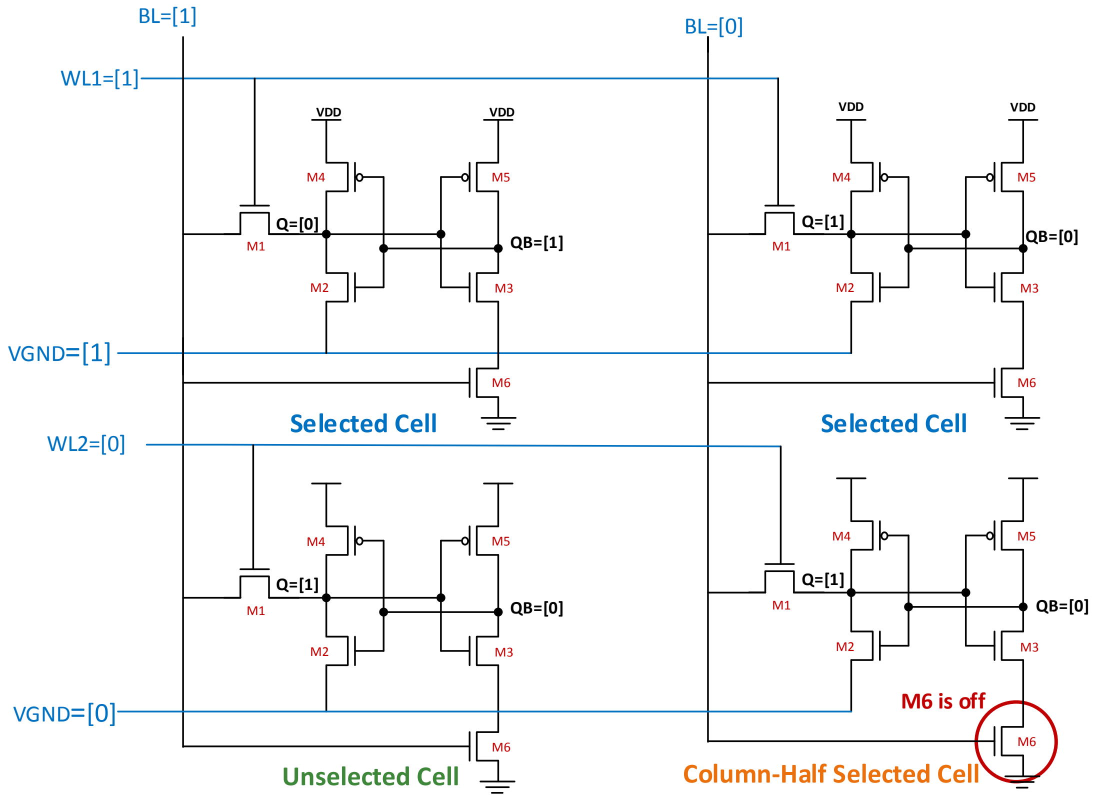


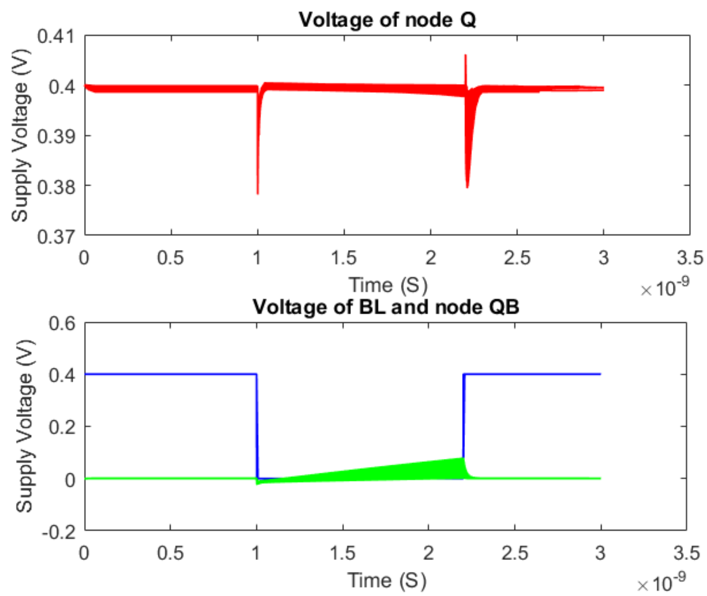
Fig. 14. Static power of compared cells (a) when Q=' 0', (b) when Q=' 1' and (c) average for different supply voltages.

$$EQM = \frac{1}{Read\ Delay \times P_{Leakage}} \times \frac{Hold\ SNM \times Read\ SNM \times Write\ SNM}{Area(Normalized\ to\ 6T) \times P_{Read} \times P_{write}} \tag{5}$$

where Hold and Read Static Noise Margins are the margins during read and hold operations. Write SNM is the write margin of the cell. Read delay is the read access time. $P_{leakage}$ is the average leakage power. P_{Read} and P_{write} are dynamic powers in the read and write operations. The area is the bit-cell area normalized to the 6T cell. The following table lists the EQM of SRAM cells at different supply voltages considered in this work. The proposed 6T SRAM cell has the highest EQM at all supply voltages. The EQM of the proposed 6T SRAM cell, at V_{DD} = 0.4 V, is 10x, 3.2x, 14.6x, 3.74x, 17.2x, and 16.75x compared to the cells 6T, WRE8T, ST-1, SB9T, 10T, and 12T, respectively. Due to the overall performance along with the least amount of area overhead, the proposed 6T SRAM cell is an attractive choice.



(a)



(b)

Fig. 15. The circuit configurations (a) Column Half-Select, (b) Monte Carlo simulations for Column Half-select.

Table 3. Layout area for different cells.

Cell Structures	Length (λ)	Width (λ)	Area (λ^2)	Normalized to 6T
6T	55	16	880	1
WRE8T	54	24	1296	1.47
SB9T	74	24	1776	2.02
Proposed 6T	**55**	**18**	**990**	**1.125**
ST-1	76	24	1824	2.07
12T	101	16	1616	1.84
10T	75	26	1950	2.21

Table 4. Table comparing the proposed 6T parameters to those of other structures at VDD = 0.4 V.

Parameters	6T	WRE8T	ST-1	SB9T	12T	Proposed 6T	10T
Static Power (nW)	10.8	10.2	11.4	9.6	11.4	7.25	13.8
Read Time (PS)	20	32	49	62	30	22.6	11.2
Write '0' Time (Ps)	7.6	10.4	9.4	28	7.6	11.7	6.9
Write '1' Time (Ps)	7.6	166	9.4	153	7.6	346	9.8
RSNM (V)	0.07	0.069	0.082	0.12	0.121	0.105	0.133
HSNM (V)	0.14	0.137	0.173	0.12	0.121	0.106	0.133
WSNM '0' (V)	0.086	0.196	0.096	0.056	0.196	0.185	0.156
WSNM '1' (V)	0.086	0.186	0.096	0.217	0.196	0.167	0.236
Read Energy (fJ)	7.9	8.2	9.2	14	11.2	7.28	9.1
Write Energy (fJ)	58.2	70	68	99.3	122.2	58	134
Read Power (mW)	0.4	0.26	0.19	0.22	0.36	0.32	0.81
Write '0' Power (mW)	7.7	6.7	7.2	3.6	16	4.96	19.6
Write '1' Power (mW)	7.7	0.43	7.2	0.65	15.1	0.17	13.7
Area (λ^2)	880	1296	1824	1776	1616	990	1950

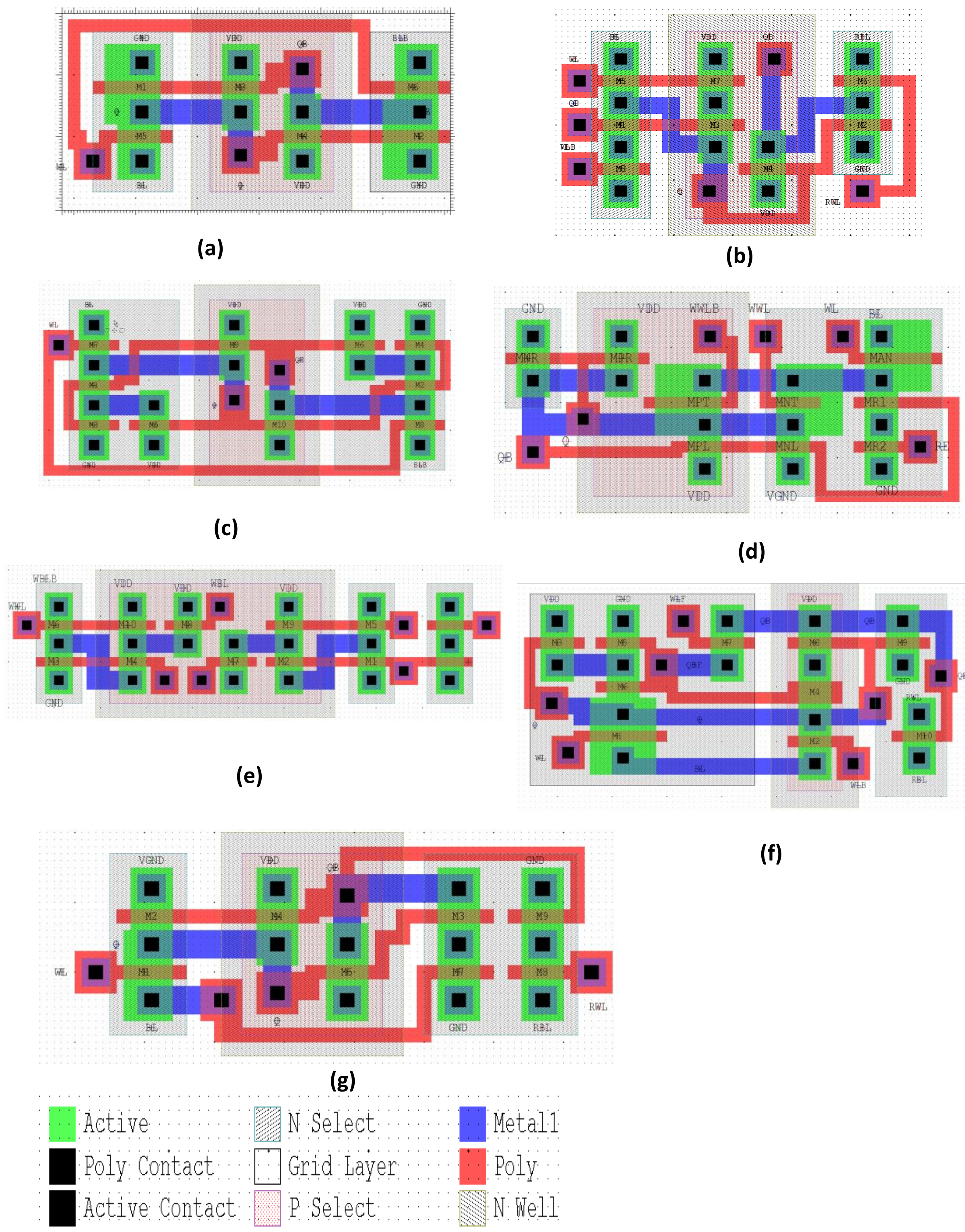


Fig. 16. The layout of (a) 6T, (b) WRE8T, (c) ST-1, (d) SB9T, (e) 12T, (f) 10T, (g) proposed 6T SRAM cells.

Table 5. EQM of different cells at different supply voltage(×1E20).

Electrical Quality Metric							
VDD	**6T**	**WRE8T**	**ST-1**	**Proposed 6T**	**12T**	**SB9T**	**10T**
400mV	12.9	40.8	8.79	**129**	7.69	34.5	7.5
500mV	3.12	7.8	2.18	**26.7**	1.69	6.4	2.05
600mV	1.02	2.04	0.89	**8.2**	0.59	2	0.76
700mV	0.4	0.59	0.4	**2.94**	0.24	0.76	0.32
800mV	0.16	0.18	0.2	**1.08**	0.11	0.33	0.15
900mV	0.063	0.057	0.1	**0.4**	0.054	0.14	0.08

4- Conclusion

A single-ended bit-interleaved SRAM cell with appropriate low power, high performance, and robustness characteristics is presented in this paper. In the write operation, the back-to-back inverters feedback is weakened by turning off the pull-down path to write the node '1'. Among the compared structures, this structure has the highest write ability. Compared to the proposed cell, SRAM cells have lower read and write energy (power) due to the single-ended structure. Despite a longer write (due to the single-ended operation), the proposed SRAM could be a striking choice for moderate throughput low power applications that require frequent readings. Compared to the related structures, the proposed structure consumes tolerable leakage power. The EQM of the proposed 6T cell compared to cells 6T, WRE8T, ST-1, SB9T, 10T, and 12T 10x, 3.2x, 14.6x, 3.74x, 17.2x, and 16.75x, respectively, at V_{DD} = 0.4 V. The future work will focus on expanding our work towards In-memory Computation (IMC) and searching for different implementations of the proposed structure for Boolean operations.

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