A Multi-Stage TIA based on Cascoded-Inverter Structures for Low-power Applications

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Abstract:

This article discusses a multi-stage transimpedance amplifier (TIA), which is based on three stages of a modified inverter structure. The traditional inverter structure's performances are improved by adding two cascoded transistors. This new structure benefits from elimination of the Miller-capacitances in comparison with the traditional inverters, which can provide higher speed and wider frequency bandwidth. Manipulating the trade-offs among bandwidth, gain and power consumption beside using G_m/I_D technique, this paper introduces a low-power transimpedance amplifier for high-bit rates in optical communication receiver systems. Moreover, active types of inductors are also used to lessen the occupied area and increase the frequency bandwidth. Transferring poles of the improved circuit to higher frequencies mean less required DC current for a fixed bandwidth range, which results in low-power characteristic.

Keywords:

Transimpedance Amplifier, Optical Frond-End, Low Power, Cascoded-Inverter, Active Inductive Peaking, G_m/I_D.

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1. Introduction

Growing demands for high data rates in communication systems obliged us to use light as the fastest signal carrier in integrated communication systems. Optical fibers, of course, are known as the best medium for carrying large volumes of data, due to their superior performance in terms of bandwidth, crosstalk, electromagnetic interference and channel loss in comparison with conventional mediums [1]. Besides, in deep-submicron CMOS technologies, the transit frequency has been increased rapidly. So, silicon integrated circuits introduce the best technology that can properly provide acceptable level of integration beside an acceptable speed and cost.

Figure (1), demonstrates the transmitter system, a medium like optical fiber, and the receiver, all together. The Transimpedance Amplifier (TIA), as the first stage of a receiver system, is the most critical building block, due to the fact that its performance affects the performance of the whole receiver system.

Travelling from the near-end to the far-end, the light might experience a considerable attenuation [1-2]. So, The TIA in the far-end must amplify the produced signal by the photodiode with low-noise and proper bandwidth, while converting it to a voltage signal. This process faces various difficulties such as the second order effects and nonlinearities of using deep sub-micron technologies, beside the existence of trade-offs among gain, bandwidth, noise, power consumption and the voltage headroom. Moreover, the photodiode, which converts the input optical signal to an electrical current signal, introduces a large parasitic capacitance in the input node of the TIA, which usually forms the dominant pole of the TIA [3-10]. Different structures are introduced in literature to compensate the effect of this large parasitic capacitance, among which some of them like Regulated-Cascode (RGC) structures are well-known [3, 11-13]. Although reported TIAs in [11-13] obtained broadband circuits, the usage of passive inductors and resistors occupy a large area on chip. Moreover, RGC structures require high voltage-headroom, when high-speed applications are of interest. In addition, in [14] a new method is used to convert transistor's transconductance to transimpedance instead of using a resistor to do this conversion. Although this method benefits from

further degree of freedom in comparison with previously published structures, the inductors used in this topology yield large occupied area on chip.

Furthermore, in [15] a π-network is employed as the TIA stage along with a folded-cascode-based shunt amplifier. Although a high-gain and low-noise structure is achieved in this technique, high power consumption and using passive inductors are counted as its drawbacks.

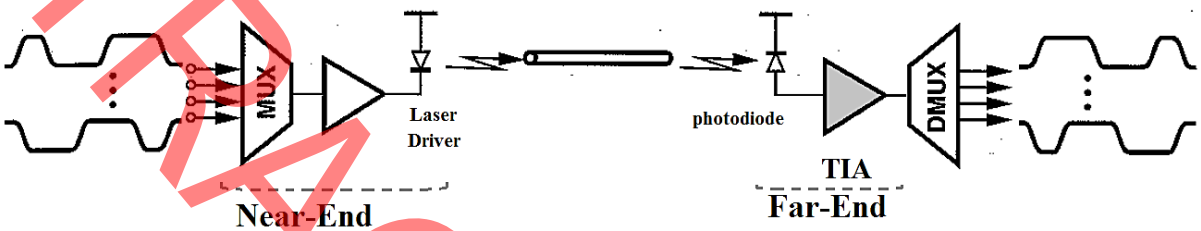


Fig 1. Introducing TIA in a transmitting and receiving system [1]

Another structure, which is widely used in designing TIAs, is the inverter [16-20]. In [16], a three-stage cascade push pull conventional inverter is used, beside series inductive peaking technique. Employing series inductive peaking results in an extended bandwidth, while occupies large area on chip. Moreover, in [17], an inverter with a diode connected NMOS and a cascoded PMOS load is proposed. This structure benefits from a wide dynamic range, whose bandwidth is limited to only 227MHz. Also, in [18] a conventional inverter structure is used with an active feedback, which uses an extra gain stage, while, in [19] a similar structure employs an inverter at its input stage, which is followed by a 1.5KΩ feedback resistor. Of course, implementing an integrated 1.5KΩ resistor occupies a considerable area on chip. In addition, in [19] a conventional inverter is used as the booster of an RGC, which isolates the parasitic capacitance of the photodiode, by lowering the input impedance, while, suffers from the miller capacitance in the inverter stage.

Generally speaking, the conventional structure of the inverter structure suffers from the Miller capacitance. Let's take a look at figure (2). Gate-drain capacitance of the PMOS and gate-drain capacitance of the NMOS in a conventional inverter, introduce the Miller capacitance, which extremely limits the speed, data rate, and bandwidth in these structures. This yields the main drawback of the conventional inverters.

In this paper, in order to omit the miller capacitance in conventional inverter structures, a cascoded version of the inverter is employed. Moreover, to obtain higher transimpedance gain, three stages of the cascoded-inverter is used in series. Furthermore, in order to extend the frequency bandwidth, active types of inductors are employed, which in comparison with passive inductors save the chip area.

Also, using cascoded-inverter results in less DC current passing through the circuit, which yields less power dissipation. Of course, this less power dissipation is achieved in cost of less output voltage swing.

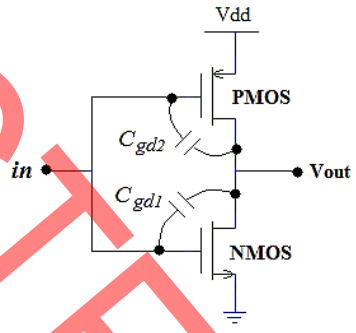


Fig 2. realization of the Miller capacitance in a conventional Inverter structure

So, in order to increase the swing, an output stage is added. The output stage, which employs an active inductor, not only provides proper output swing, but also resonates with the capacitive load and provides extra frequency bandwidth. Also, in designing the proposed TIA, the g_m/I_D technique [21-24] is used to properly extract the ratio of width and length of each transistor in 90nm CMOS technology. This method provides a clear vision for the designer and hence a useful way to estimate dimensions of transistors [24]. As choosing proper dimension is a challenging task in designing low-power circuits, the g_m/I_D method can be very useful for this purpose, since the designer is capable of choosing the dimension of transistors in a moderate region, so that a proper trade-off between speed and the power can be obtained. The presented circuit in this paper is suitable for low-power, 5Gbps optical communication systems, in which a proper trade-off is maintained for this purpose using g_m/I_D technique.

So, the organization of this paper is as so. In section (2), the proposed CI TIA structure is introduced and its behavior is mathematically discussed. Section (3) deals with extracting the proper transistor dimensions using g_m/I_D method. Simulation results and analysis are given in section (4), while, section (5) gives the noise analysis. Finally, section (6) concludes the paper.

2. The proposed TIA

Figure (3-a) demonstrates the proposed transimpedance amplifier building block, while the circuit schematic of the proposed TIA is shown in figure (3-b). As it is shown in figure (3-a), a three-stage cascoded inverter is used in a closed-loop circuit as the first stage of the amplifier. For further amplification a post amplifier is used employing an active type of inductor, which is followed by a buffer.

The cascoded-inverter structure benefits from the absence of the Miller capacitance, as it is discussed before. Employing M3 and M4 at the first stage of the inverter (also M13-M14 at the 2nd stage, and M23-M24 at the 3rd stage) avoid a direct connection between the input node and the output node, so the Miller effect is no longer a restriction. Moreover, combination of M5-M6 (also, M25-M26) provides an active type of inductor [1,7], which starts to resonate with the parasitic capacitances of the nodes *out1* (and *out3*) as frequency increases. Hence, a faster structure with higher data rate and a wider frequency bandwidth can be obtained. Using M15 as a diode-connected load at node *out2*, provides a trade-off between the gain and the bandwidth [16]. M15 acts as the load of the second inverter stage. Currents produced by M11 and M12 are multiplied by (1/gm15) as a resistor, and the output voltage is obtained. Hence the higher the (1/gm15), the more the gain. On the other hand, this is approximately the output resistance, which forms a pole. Hence the higher the (1/gm15), the less the bandwidth. And that reveals the trade-off.

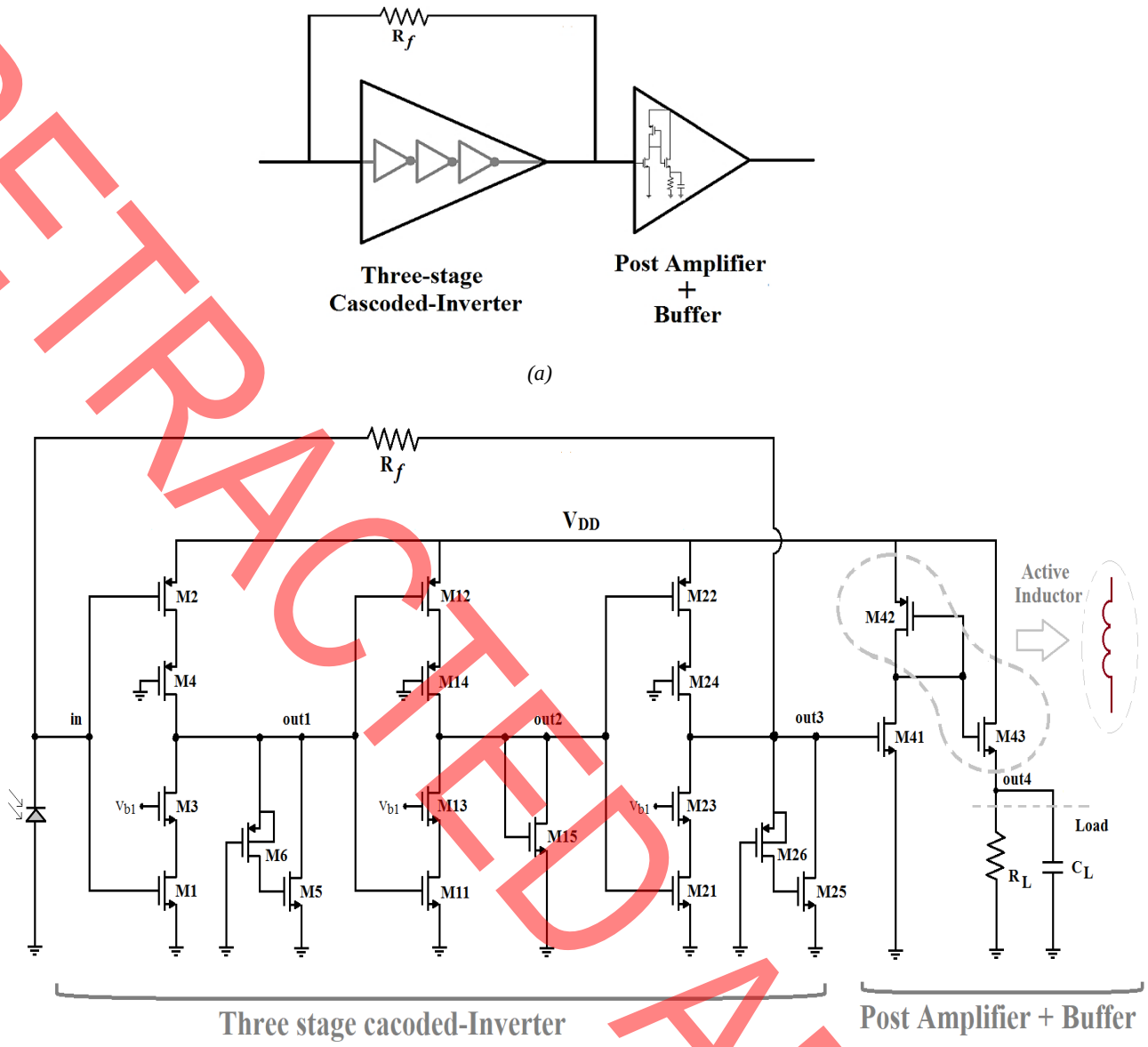


Fig 3. The Proposed TIA, (a) building block, (b) The proposed circuit

By changing the width of M15, the bandwidth at node *out2* can be set. These three cascoded-inverter structures are cascaded in a closed loop. Furthermore, for further amplification a gain stage is used employing a diode-connected load, which is followed by buffer stage. The combination of M42 as the diode connected transistor with the buffer forms an active inductor (through the gate-source capacitance of M43), which resonates with the load capacitance and moves the output pole to higher frequencies. So, in order to obtain a specified data rate, less DC current is required to pass through the circuit.

As there will be several stages of limiting amplifiers (LAs) after the TIA stage in an optical receiver, wide swing outputs are not needed to be obtained at the TIA stage, but they are needed to be obtained at the LA stages. That is why most LA stages are differential-based amplifiers.

As the main challenge in designing TIAs is their dominant pole due to the high parasitic capacitance of the photodiode, the input resistance in this design is reduced using a proper voltage-current feedback. Hence, the feedback network moves the dominant pole to higher frequencies, as well. Also, it is worth noting that similar to conventional inverters, the cascoded-inverter base TIA exhibits less input referred noise, due to the summation of merely two transconductances (g_{m1}+g_{m2}).

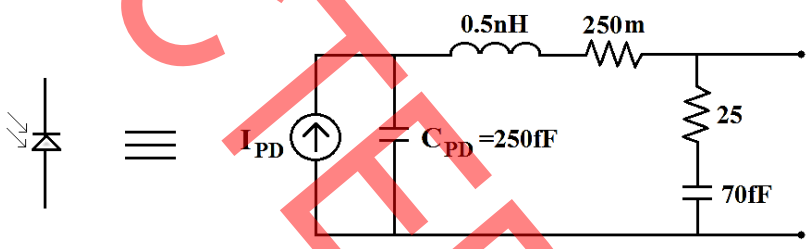


Fig 4. Equivalent circuit of the photodiode

In addition, figure (4) demonstrates the equivalent circuit used as the photodiode [25, 26].

In order to analyze the proposed circuit, let's start with analyzing the transimpedance gain of the circuit structure. The transconductance of each cascoded-inverter stage is defined with g_m, and the total transconductance of the three-stage cascode-inverter can be defined as follows:

$$G_{m,total} = A_{V1} \times A_{V2} \times G_{m3} \quad (1)$$

In which, A_v represents the voltage gain, G_m represents the transconductance of the i^{th} cascoded-inverter stage that are defined as follows:

$$G_{m1} = g_{m1} + g_{m2} \quad (2)$$

$$G_{m2} = g_{m11} + g_{m12} \quad (3)$$

$$G_{m3} = g_{m21} + g_{m22} \quad (4)$$

Where, g_m is the transconductance of a MOSFET transistor.

Moreover, the resistance seen at nodes *out1* and *out2* can be defined as follows:

$$R_{out1} = \{[1 + (g_{m3} + g_{mb3})r_{o3}]r_{o1} + r_{o3}\} \| \{[1 + (g_{m4} + g_{mb4})r_{o4}]r_{o2} + r_{o4}\} \| Z_{D1} \quad (5)$$

$$R_{out2} = \{[1 + (g_{m13} + g_{mb13})r_{o13}]\, r_{o11} + r_{o13}\} \| \{[1 + (g_{m14} + g_{mb14})r_{o14}]r_{o12} + r_{o14}\} \| \frac{1}{g_{m15}} \quad (6)$$

In which, R_{out1} is the resistance seen at node (*out1)*, r_o is the drain-source resistance of a MOSFET, g_{mb} represents the bulk effect and Z_{D1} is the impedance of combination M5-M6 as an active inductor, as follows [1]:

$$Z_{D1} = \frac{\frac{1}{g_{m6}}.C_{gs5}.S+1}{g_{m5}+C_{gs5}.S} \quad (7)$$

In which, C_{gs} is the gate-source capacitance of the MOSFET and the active inductor can be derived from equation (7), as follows:

$$L = \frac{C_{gs5}}{g_{m5}}\left(\frac{1}{g_{m6}} - \frac{1}{g_{m5}}\right) \quad (8)$$

It is obvious from equation (7), that at low frequencies the combination of M5-M6 acts as a diode-connected transistor, as follows:

$$\lim_{S\to 0} Z_{D1} = \lim_{S\to 0} \frac{\frac{1}{g_{m6}}.C_{gs5}.S+1}{g_{m5}+C_{gs5}.S} = \frac{1}{g_{m5}} \quad (9)$$

So, without considering the feedback network R_{out3} can be written as follows:

$$R_{out3} = \{[1 + (g_{m23} + g_{mb23})r_{o23}]r_{o21} + r_{o23}\} \| \{[1 + (g_{m24} + g_{mb24})r_{o24}]r_{o22} + r_{o24}\} \| Z_{D2} \quad (10)$$

In which:

$$Z_{D2} = \frac{\frac{1}{g_{m26}}.C_{gs25}.S+1}{g_{m25}+C_{gs25}\,.\,S} \quad (11)$$

By considering equation (7) and (9) and considering the fact that the feedback network is sampling the voltage at node *out3*, and also considering that $[1+(g_{m3}+g_{mb3})r_{o3}]r_{o1}+r_{o3} \gg {}^{1}/_{g_{m5}}$ and $[1+(g_{m4}+g_{mb4})r_{o4}]r_{o2}+r_{o4} \gg {}^{1}/_{g_{m5}}$, equations (5), (6) and (10) at low frequencies can be simplified as follows:

$$R_{out1} \approx \frac{1}{g_{m5}} \tag{12}$$

$$R_{out2} \approx \frac{1}{g_{m15}} \tag{13}$$

$$R_{out3} \approx \frac{1}{g_{m25}\left(1+\frac{1}{R_f}A_{Z,TCI}\right)} \tag{14}$$

Where R_f represents the feedback network and $A_{Z,TCI}$ represents the transimpedance gain of the Three-stage Cascoded-Inverter (TCI) stage.

Moreover, the gain of the common source (CS) amplifier as the post amplifier can be written as follows:

$$A_{V,CS} = g_{m41}.\frac{1}{g_{m42}} \tag{15}$$

And for the gain of the buffer stage, it can be written as follows:

$$A_{V,Buffer} = \frac{g_{m43}\,R_L}{1+(g_{m43}+g_{mb43})R_L} \tag{16}$$

Furthermore, as the dominant pole is usually formed at the input node of the TIAs, it is vital to reduce the input resistance to compensate the effect of the large parasitic capacitance of the photodiode. So, here a proper feedback structure is used, which reduces the input resistance of the proposed TIA. Hence, the input resistance of the proposed circuit structure can be written as follows:

$$R_{in,f} = \frac{R_f}{1+\frac{1}{R_f}(A_{Z,TCI})} \tag{17}$$

And for the output node it can be written as follows:

$$R_{out} = \frac{1}{g_{m43}+g_{mb43}} \| R_L \tag{18}$$

While for the input and output capacitances it can be written as follows:

$$C_{in} = C_{Pd} + C_{gs1} + C_{gs2} + C_{gd1} + C_{gd2} \tag{19}$$

$$C_{out} = C_L + C_{gs43} + C_{gd43} \tag{20}$$

In which C_{Pd} is the parasitic capacitance of the photodiode, C_{gd} is the gate-drain parasitic capacitance, C_{gb} is the gate-bulk parasitic capacitance of a MOSFET and C_L is the load capacitance. As C_{Pd} is relatively large, C_{in} can be approximated to be equal to C_{Pd}.

Moreover, for the parasitic capacitances at *out1*, *out2* and *out3*, it can be written as follows:

$$C_{out1} = C_{gs11} + C_{gd11} + C_{gs12} + C_{gd12} + C_{dg5} + C_{gs6} + C_{ds5} + C_{dg4} + C_{dg3} + C_{ds3} + C_{ds4} \quad (21)$$

$$C_{out2} = C_{gs21} + C_{gs22} + C_{gd21} + C_{gd22} + C_{ds15} + C_{dg13} + C_{dg14} + C_{ds13} + C_{ds14} \quad (22)$$

$$C_{out3} = C_{gs41} + C_{gd25} + C_{ds25} + C_{gs26} + C_{dg23} + C_{dg24} + C_{ds23} + C_{ds24} \quad (23)$$

Where, C_{gd} is the drain-gate capacitance of a MOSFET.

So, by considering the above mentioned facts, the transfer function of the three stage cascoded-inverter (TCI), which consists of six poles and one zero, can be written as follows:

$$A_{V,TCI} = G_{m1}.G_{m2}.G_{m3}.R_{out1}.R_{out2}.R_{out3}$$

$$A_Z(s) = A_{Z,TCI} \times A_{V,Post\ Amp.} = \frac{A_{V,TCI}}{1+A_{V,TCI}\frac{1}{R_f}} \times \frac{g_{m41}\left(\frac{C_{gs43}}{g_{m42}}.S+1\right)\times g_{m43}.R_L}{D} \quad (24)$$

Where the denominator is equal to:

$$D = (1 + C_{in}R_{in}.S)(1 + C_{out1}R_{out1}S)(1 + C_{out2}R_{out2}S)(1 + C_{out3}R_{out3}S)\big(g_{m43} + C_{gs43}S\big)[1 + (g_{m43} + g_{mb43})R_L](1 + C_{out}R_L.S) \quad (25)$$

Where the dimension of $A_{Z,TCI}$ is Ohm and the $A_{V,Post\ Amp.}$ is non-dimensional, hence $A_Z(s)$ is defined according to Ohm.

The poles and the only zero of the CI-TIA are listed as follows:

$$S_1 = -\frac{g_{m43}}{C_{gs43}} \quad (26)$$

$$S_2 = -\frac{1}{C_{out1}R_{out1}} \approx -\frac{g_{m5}}{C_{out1}} \quad (27)$$

$$S_3 = -\frac{1}{C_{out2}R_{out2}} \approx -\frac{g_{m15}}{C_{out2}} \quad (28)$$

$$S_4 = -\frac{1}{C_{out3}R_{out3}} \approx -\frac{g_{m25}\left(1+\frac{1}{R_f}A_{Z,TCI}\right)}{C_{out3}} \quad (29)$$

$$S_5 = -\frac{1}{C_{in}R_{in}} \approx -\frac{1+\frac{1}{R_f}\left(A_{Z,TCI}\right)}{R_f\,(C_{Pd})} \quad (30)$$

$$S_6 = -\frac{1}{C_{out}R_L} \quad (31)$$

$$Z_1 = -\frac{g_{m42}}{C_{gs43}} \quad (32)$$

S_1, S_2, S_3 and S_4 are not in operational frequency range of the TIA, due to their significantly small capacitance. Z_1 is set to resonate with S_6 and to compensate its effect. So, by a good approximation the transfer function of the proposed TIA can be written as a first order function. Hence, for the frequency bandwidth of the proposed TIA, it can be approximately written as follows:

$$f_{-3dB} \approx \frac{1+\frac{1}{R_f}.A_{Z,TCI}}{2\pi.C_{Pd}.R_f} \quad (33)$$

In the next section, designing the proposed TIA structure with g_m/I_D technique is given.

3- g_m/I_d Technique

Designing Nano-meter CMOS circuits according to the "square-Law" equation is inaccurate and requires lots of iterations in simulators to obtain proper results. g_m/I_D technique makes it possible to change the design variables from transistor dimensions (length and width) to the value of drain current and values of g_m/I_D parameters.

The g_m/I_D characteristic curve for NMOS and PMOS are generated for 90nm CMOS technology, which is shown in figure (5). Figure (5) demonstrates the relationship between the transconductance and the normalized current (I_n), in which $I_n=I_D/(W/L)$, while, both axes in figure (5) are independent of transistor dimensions.

As it is required to obtain a proper bandwidth beside an adequate gain, most of the transistors are chosen to be in moderate, except those which are supposed to operate in triode region such as M6 and M26. Three stages of the inverter (M1, M2, M11, M22, M21, M22) are supposed to provide gain, with high data rates, so a small g_m/I_D is assigned for them in moderate inversion. The PMOS M4, M14 and M24 are used as cascoded structures to isolate the Miller capacitance of conventional structures as discussed before, they are assigned to operate at strong inversion, while NMOS M3, M13 and M23 are used to obtain gain and speed, and so moderate inversion is chosen for them.

Table (1), provides the operation region and DC current budget for each transistor. Moreover, as M6 and M26 are supposed to operate in deep triode region as resistors and no current is supposed to pass through gates of M15 and M25, the small rate of 10 is chosen for $(W/L)_{15}$ and $(W/L)_{25}$. So, after choosing the value of g_m/I_D, I_n can be extracted from figure (5) and so by assigning a DC current budget for each branch, the W/L ratio for each transistor can be obtained. It is assumed that in order to obtain a 2.5mW power consumption using 1V supply, 2500µA must be divided into the 5 existing branches, which yields 500µA DC current (I_D) passing through each branch.

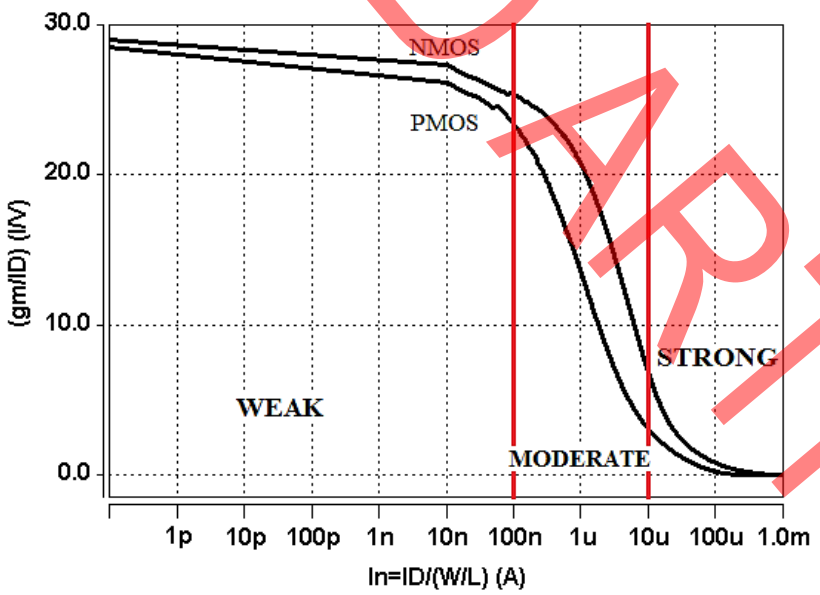


Fig 5. The extracted g_m/I_D curve for 90nm CMOS technology

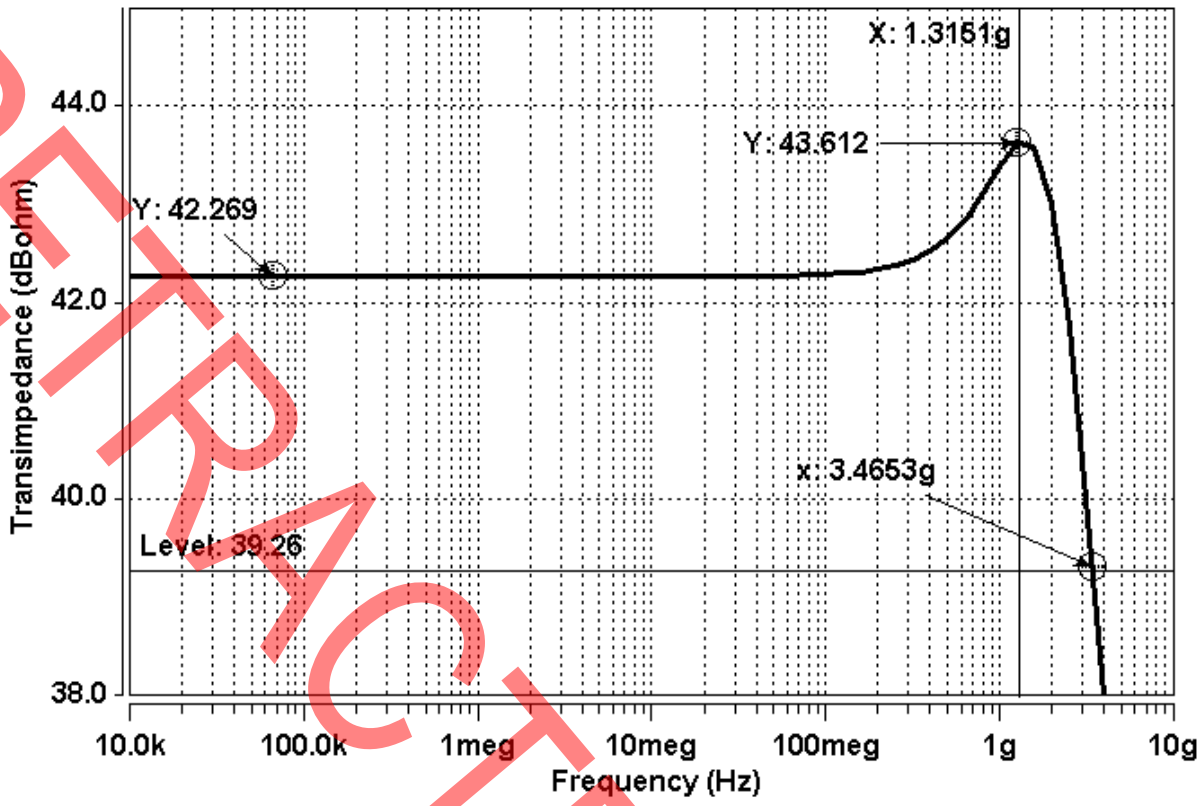
Table 1. Extracting W/L using g_M/I_D

No. of Transistor	Type of Transistor	Type of Inversion	Value of g_m/I_D	DC current Budget (I_D)	Normalized Current (I_n)	$\frac{W}{L}$
M1	NMOS	Moderate	10	500µA	7.5nA	66
M2	PMOS	Moderate	5	500µA	5.6µA	88
M3	NMOS	Moderate	15	250µA	2.3µA	88
M4	PMOS	Strong	1	250µA	37.8µA	6
M5	NMOS	Moderate	16	250µA	2.25µA	16
M11	NMOS	Moderate	10	500µA	7.5nA	66
M12	PMOS	Moderate	5	500µA	5.6µA	88
M13	NMOS	Moderate	15	250µA	2.3µA	88
M14	PMOS	Strong	1	250µA	37.8µA	6
M15	NMOS	Moderate	16	250µA	2.25µA	100
M21	NMOS	Moderate	10	500µA	7.5nA	66
M22	PMOS	Moderate	5	500µA	5.6µA	88
M23	NMOS	Moderate	15	250µA	2.3µA	88
M24	PMOS	Strong	1	250µA	37.8µA	6
M25	NMOS	Moderate	16	250µA	2.25µA	111
M41	NMOS	Moderate	16	500µA	2.5µA	200
M42	PMOS	Moderate	5	500µA	5.6µA	88
M43	NMOS	Moderate	16	500µA	2.25µA	222

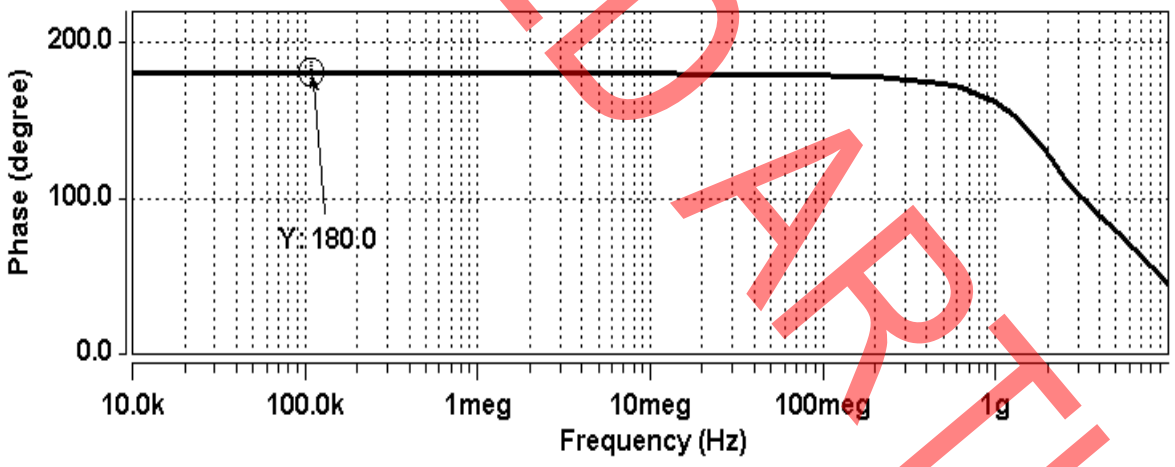
4- Simulation Results

To verify the suitable performance of the proposed CI-TIA using obtained dimensions in the previous section, the proposed circuit is simulated using 90nm CMOS technology parameters. Results for frequency response is shown in figure (6-a). As it can be seen, simulations show the transimpedance gain of 42.3dBΩ and the bandwidth of 3.47GHz. Moreover, the circuit consumes 2.7mW using 1V supply, which is relatively close to the targeted 2.5mW power, discussed in previous section. As it can be seen in figure (6-a), a peaking of about 1.3dB has occurred at high frequencies, which proves the proper performance of the active inductor. Moreover, figure (6-b) shows the phase response of the TIA starts from +180º, which yields the existence of a zero before the dominant pole in the transfer function of the TIA. As there will be several stages of limiting amplifiers (LAs) after the TIA stage in an optical receiver, the overall peaking of the receiver system will be considerably reduced.

Furthermore, the eye diagram of the CI-TIA is simulated using a 150µA input signal with NRZ PRBS23. The eye diagram is shown in different nodes of *out1*, *out2*, *out3* and the output of the TIA (*out4*) in figure (7). As it can be seen in figure (7), a bias voltage of about 420mV to 430mV is upon nodes *out1*, *out2* and *out3*. The eye is opened about 5mV at *out1*, about 10mV at *out2*, 20mV at *out3* and about 25mV at output of the TIA.



(a)



(b)

Fig 6. (a) Frequency response and (b) the phase response of the CI-TIA

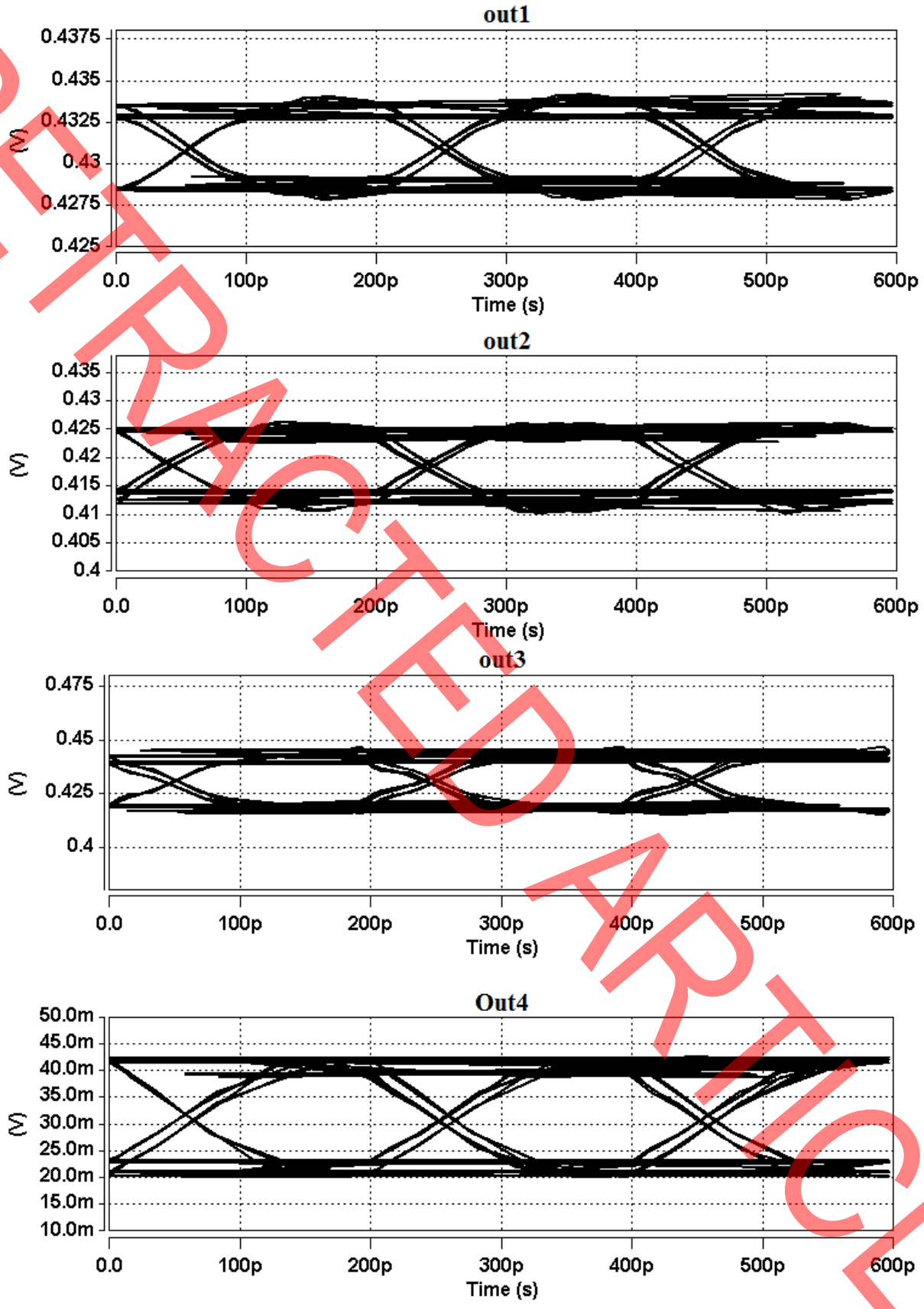
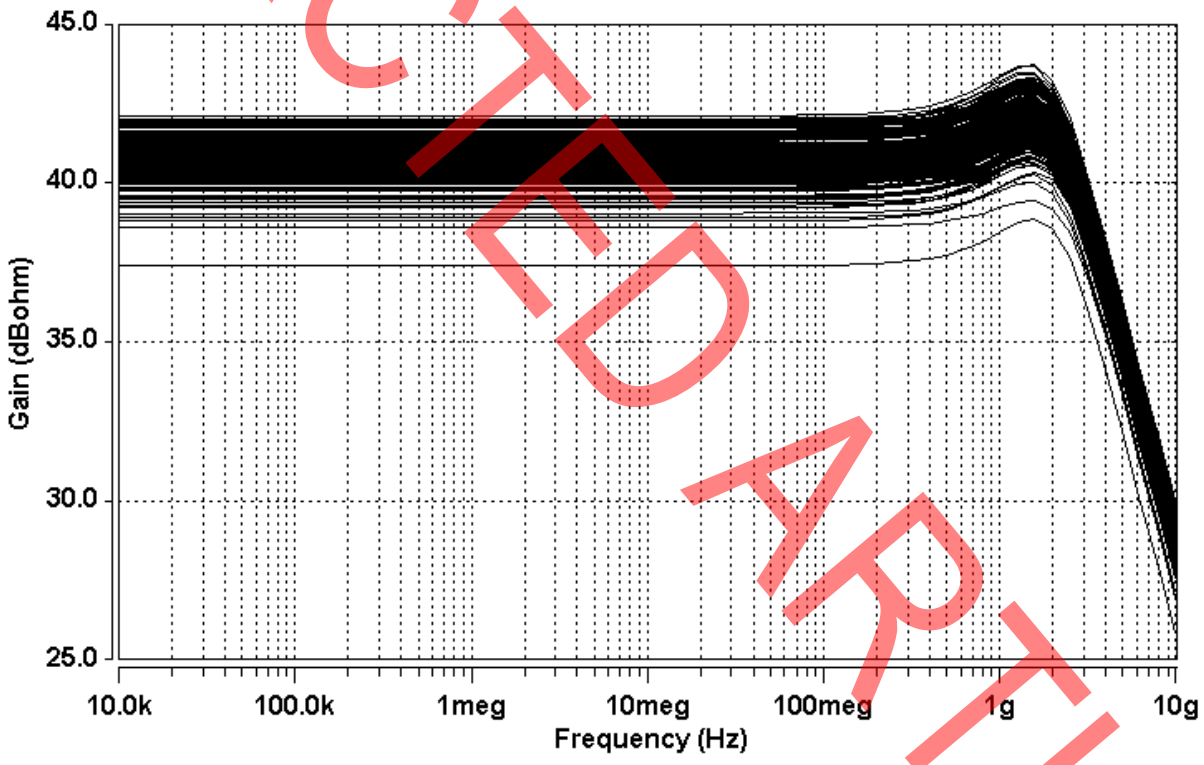


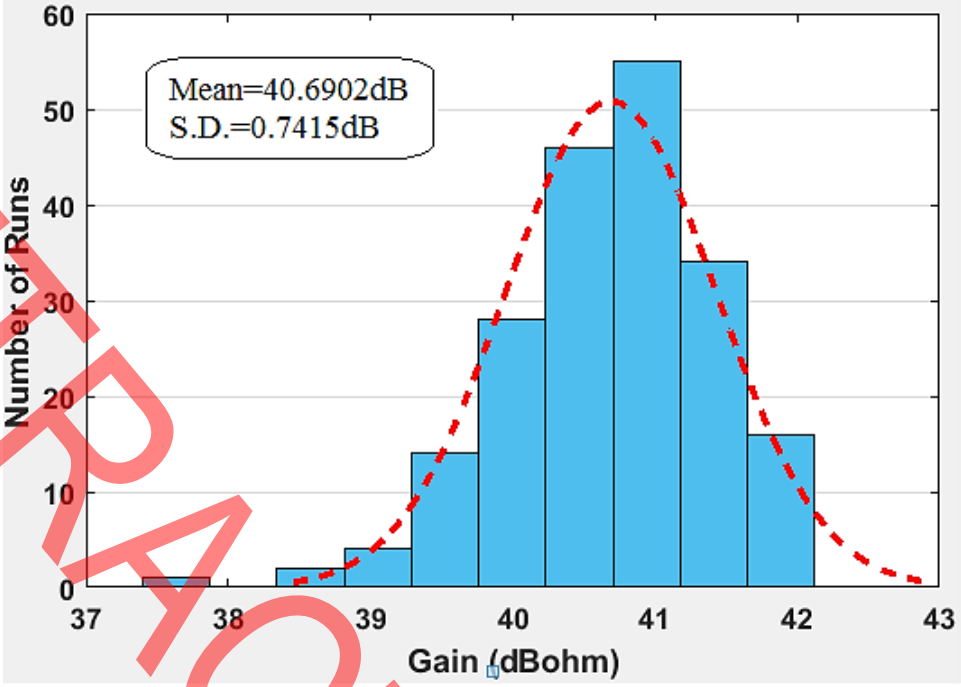
Fig 7. demonstration of the simulated eye-diagram using 150μA NRZ PRBS23 input signal at different nodes (a)out1 (b)out2 (c)out3 and (d)out4

In addition, MONTECARLO analysis (process analysis) is done in order to analyze the fabrication process. Figure (8-a) demonstrates the MONTECARLO for 200 runs over frequency response, while the variation of transimpedance gain in fabrication process is shown in figure (8-b), which shows the mean value of 40.7dB and standard deviation of 0.74dB.

Furthermore, as the input resistance (R_{in}) of the TIA is an effective factor in frequency bandwidth of the TIA, the input resistance and magnitude of input impedance of the proposed TIA over frequency is shown in figure (9). As it can be seen, the value of R_{in} is equal to 183Ω at low frequencies, while decreases to 55.4Ω at -3dB frequency bandwidth.



(a)



(b)

Fig 8. MonteCarlo Analysis over (a) frequency response (b) transimpedance gain

Additionally, it is worth analyzing the effect of feedback network on the value of R_{in} for the CI-TIA. As it was discussed before, the proper voltage-current feedback used in the proposed TIA reduces the input resistance. So, figure (10) compares the input resistance of the CI-TIA with & without the feedback network. As it can be seen in figure (10), the value of the R_{in} for the open-loop TIA is 5.5 times greater than the closed-loop CI-TIA.

Additionally, the effect of %10 supply voltage variations on frequency response is analyzed and the results are shown in figure (11). Table (2) summarizes this effect on the value of bandwidth, transimpedance gain and the maximum peaking. As it can be concluded, increasing V_{DD} results in a small increase in the value of gain, while significantly decreases the frequency bandwidth. Furthermore, less peaking on frequency response comes with an increased V_{DD}.

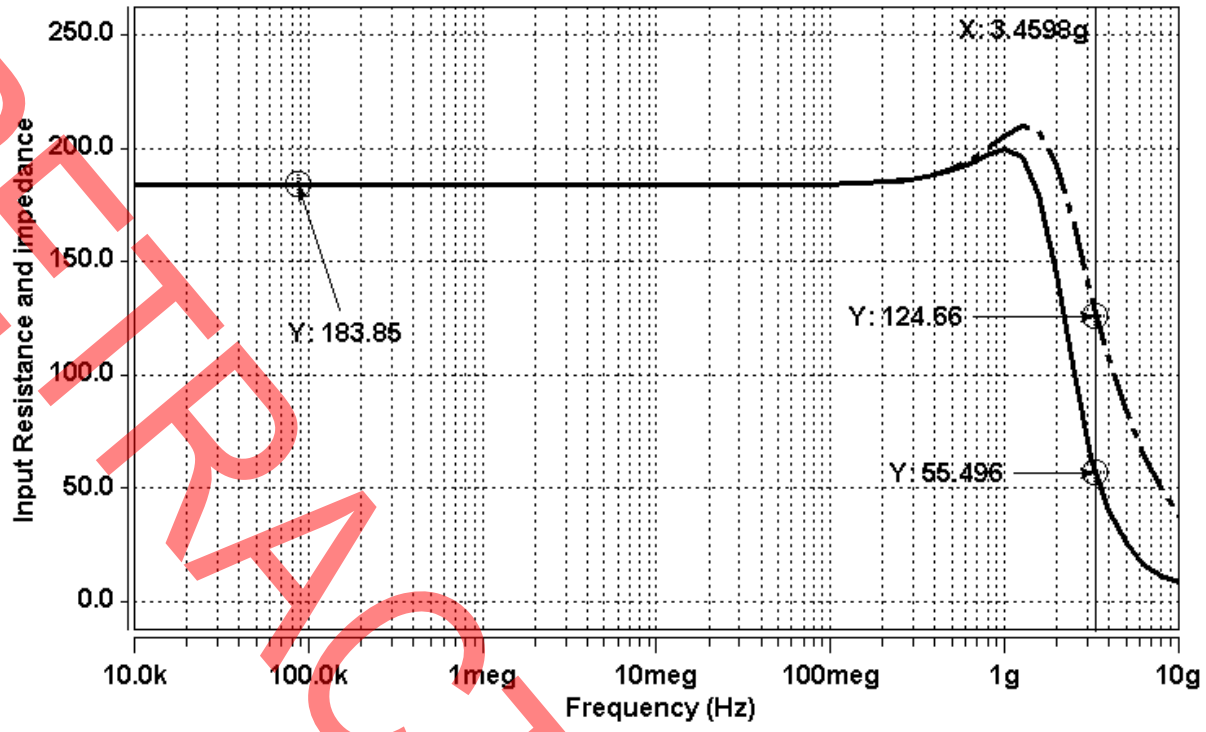


Fig 9. Input impedance and resistance

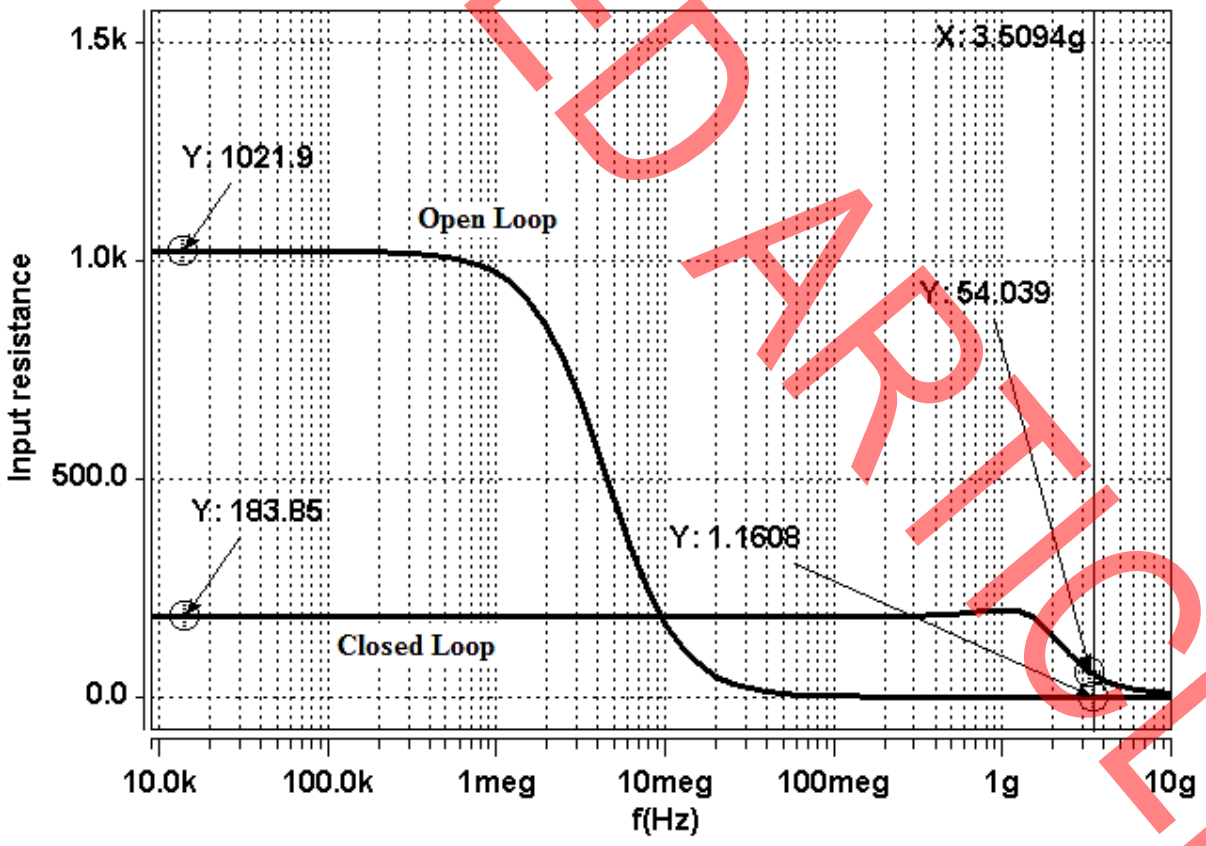


Fig 10. Input resistance with & without the feedback network

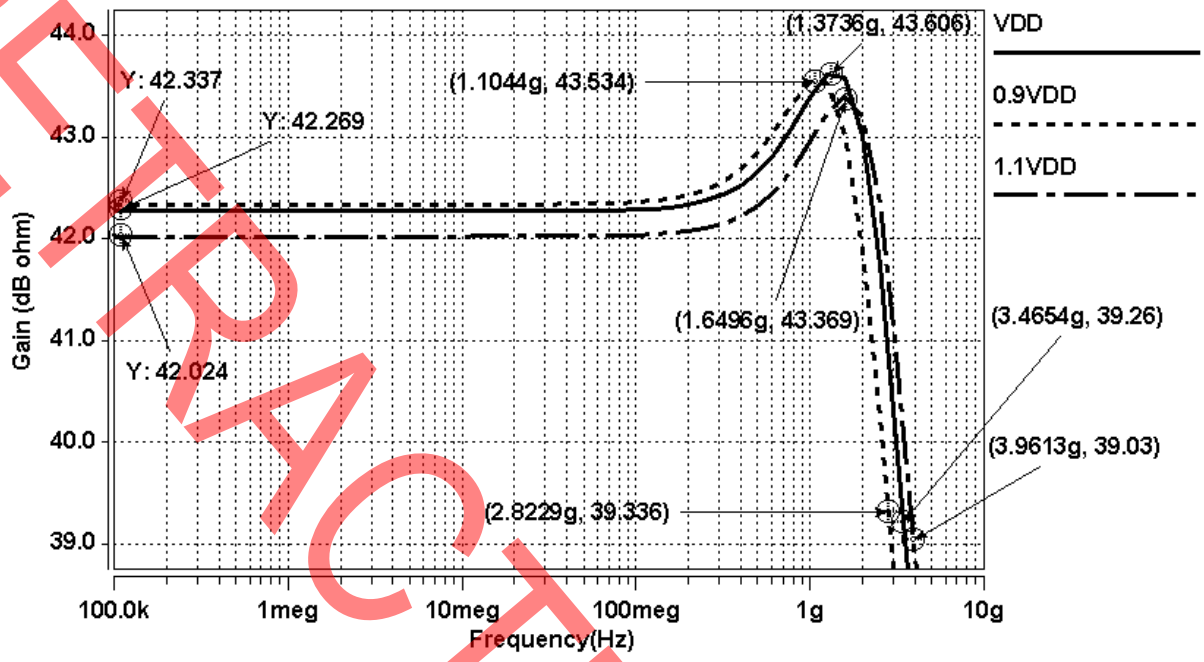


Fig 11. supply voltage variations Vs. frequency response

Table 2 Supply voltage variations on Gain, bandwidth and maximum peaking

	$0.9V_{DD}$	VDD	$1.1V_{DD}$
Gain (dBΩ)	42.02	42.3	42.33
Bandwidth	3.96GHz	3.47GHz	2.82GHz
Max. Peaking	1.4dB	1.3dB	1.2dB

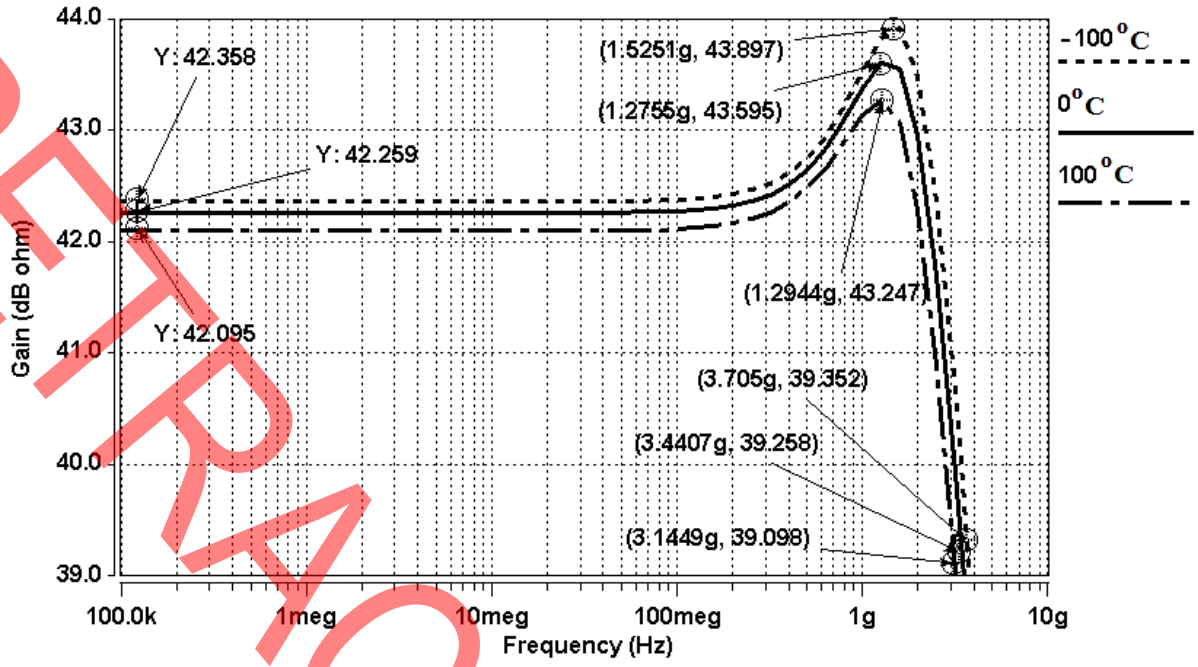


Fig 12. Temperature variations Vs. frequency response

Table 3 Temperature variations on maximum peaking, Gain and Bandwidth

	-100ºC	0ºC	+100ºC
Gain (dBΩ)	42.35	42.25	42.95
Bandwidth	3.70GHz	3.44GHz	3.14GHz
Max. Peaking	1.54dB	1.33dB	1.15dB

Moreover, the maximum peaking variations, frequency bandwidth, and transimpedance gain, according to temperature variations from -100ºC to +100ºC are analyzed and shown in figure (12). Table (3) analysis this effect numerically. As in table (3), 200ºC temperature variations results in only 0.6dB variation, while the bandwidth varies for 560MHz. Furthermore, it is shown that the height of peaking increases at lower temperatures.

5- Noise Analysis

The noise source of for each transistor is modeled with a current source in parallel, as it is shown in figure (13), to analyze the noise performance of the proposed CI-TIA.

For a simpler analysis, three equivalent noise sources in the building block of the TIA are shown as in figure (14): in the feedback network, core of the TIA [1] and in the second amplifier stage. So, the equivalent input noise value for the proposed TIA structure can be written as follows [1]:

$$\overline{I_{n,in}^2} = \frac{4KT}{R_f} + \frac{\overline{V_{n,Core}^2}}{R_f^2} + \frac{\overline{V_{n,2nd\ Stage}^2}}{\left|A_{Z,TCI(s)}\right|^2} \qquad (34)$$

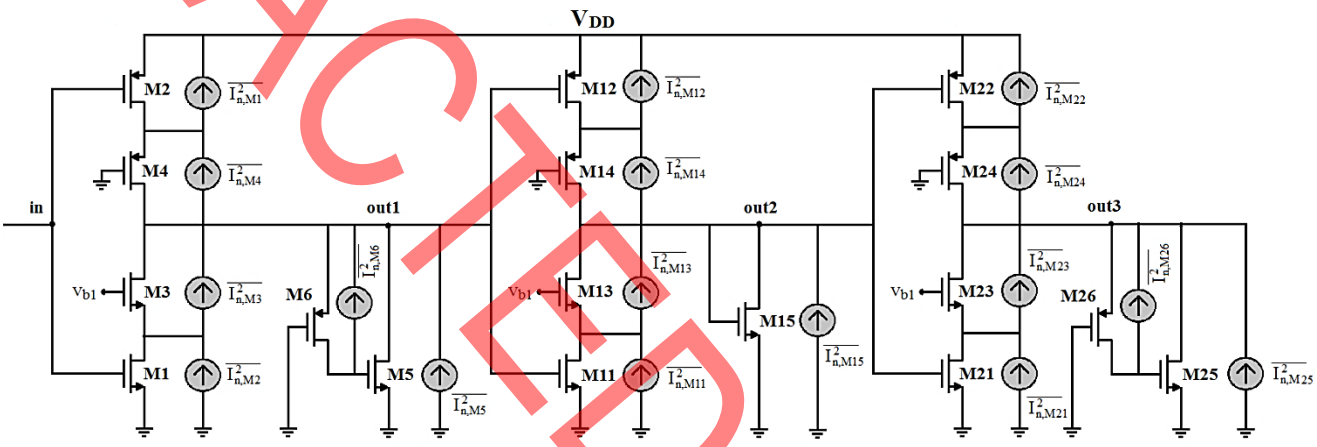


Fig 13. Demonstration of noise sources in the CI-TIA

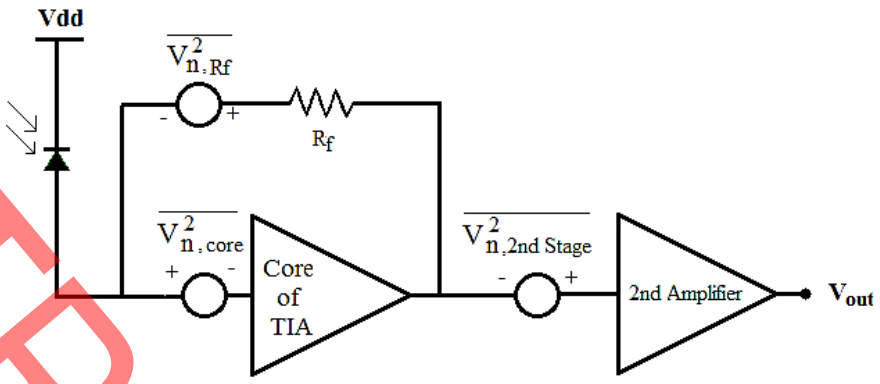


Fig 14. Equivalent noise sources of the TIA

In which $A_{Z(s)}$ is the gain of the three-stage cascoded-inverter.

As the magnitude of $A_{Z(s)}$ is relatively large it can be said that $\frac{\overline{V_{n,2nd\ Stage}^2}}{|A_{Z,TCI(s)}|^2} \ll \frac{4KT}{R_f} + \frac{\overline{V_{n,Core}^2}}{R_f^2}$. So, equation (34) can be simplified to:

$$\overline{I_{n,in}^2} \approx \frac{4KT}{R_f} + \frac{\overline{V_{n,Core}^2}}{R_f^2} \tag{35}$$

For the noise of the first stage of the cascoded-inverter it can be written as follows:

$$\overline{V_{n,out1}^2} = \overline{I_{n,out1}^2} \times |R_{out1}|^2 \tag{36}$$

Same thing can be written for the 2nd and the 3rd stage, as well.

$$\overline{V_{n,out2}^2} = \overline{I_{n,out2}^2} \times |R_{out2}|^2 \tag{37}$$

$$\overline{V_{n,out3}^2} = \overline{I_{n,out3}^2} \times |R_{out3}|^2 \tag{38}$$

Where,

$$\overline{I_{n,out1}^2} = 4kT\gamma(g_{m1} + g_{m2}) \tag{39}$$

$$\overline{I_{n,out2}^2} = 4kT\gamma(g_{m11} + g_{m12}) \tag{40}$$

$$\overline{I_{n,out3}^2} = 4kT\gamma(g_{m21} + g_{m22}) \tag{41}$$

In which k refers to the Boltzmann constant and γ refers to the channel noise factor of a MOSFET.

By neglecting the channel length modulation for M_3 and M_4 (and also for M13-M14 and M23, M24 as well) it can be said that as these transistors are operating as cascode-stages, the same amount of current will leave the drain terminal, that enters the source terminal, and so it can be written $I_{n,M3} = I_{d,M3}$ and $I_{n,M4} = I_{d,M4}$ [27]. Hence, the thermal noise of M3, M4, M13, M14, M23 and M24 can be neglected. So, it can be said that the noise of the cascoded-inverter TIA is approximately equal to the conventional inverter structure.

In order to calculate the input referred noise of the TIA, it can be written as follows:

$$\overline{V_{n,core}^2} = \frac{\overline{V_{n,out1}^2}}{\left|\frac{(g_{m1}+g_{m2}).R_{out1}}{1+C_{in}.R_{in}.s}\right|^2} + \frac{\overline{V_{n,out2}^2}}{\left|\frac{(g_{m1}+g_{m2}).R_{out1}}{1+C_{in}.R_{in}.s}\right|^2 |(g_{m11}+g_{m12}).R_{out2}|^2} + \frac{\overline{V_{n,out3}^2}}{\left|\frac{(g_{m1}+g_{m2}).R_{out1}}{1+C_{in}.R_{in}.s}\right|^2 |(g_{m11}+g_{m12}).R_{out2}|^2 |(g_{m21}+g_{m22}).R_{out3}|^2} \quad (42)$$

The poles at nodes *out2* and *out3* were neglected for simplicity.

As $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_{11} = \left(\frac{W}{L}\right)_{21}$ and $\left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_{12} = \left(\frac{W}{L}\right)_{23}$, equation (42) can be simplified due to the fact that $g_{m1} = g_{m11} = g_{m21}$ and $g_{m2} = g_{m12} = g_{m22}$, as follows:

$$\overline{V_{n,core}^2} \approx \frac{\overline{V_{n,out1}^2}}{\left|\frac{(g_{m1}+g_{m2}).R_{out1}}{1+C_{in}.R_{in}.s}\right|^2} + \frac{\overline{V_{n,out2}^2}}{\left|\frac{(g_{m1}+g_{m2})^2.R_{out1}}{1+C_{in}.R_{in}.s}\right|^2 |R_{out2}|^2} + \frac{\overline{V_{n,out3}^2}}{\frac{(g_{m1}+g_{m2})^6}{|1+C_{in}.R_{in}.s|^2}|R_{out1}.R_{out2}.R_{out3}|^2} \quad (43)$$

Hence by putting equations (36) to (41) into equation (43), it can be obtained as follows:

$$\overline{V_{n,core}^2} \approx \frac{4kT\gamma}{(g_{m1}+g_{m2})}\left[1 + \frac{1}{{R_{out1}}^2(g_{m1}+g_{m2})^2} + \frac{1}{(g_{m1}+g_{m2})^4 |R_{out1}.R_{out2}.|^2}\right](1+C_{in}.R_{in}.s)^2 =$$

$$\frac{4kT\gamma}{(g_{m1}+g_{m2})}\left[1 + \frac{1}{{R_{out1}}^2(g_{m1}+g_{m2})^2} + \frac{1}{(g_{m1}+g_{m2})^4 |R_{out1}.R_{out2}.|^2}\right] + \frac{16\pi^2 kT\gamma}{(g_{m1}+g_{m2})}\left[1 + \frac{1}{{R_{out1}}^2(g_{m1}+g_{m2})^2} + \frac{1}{(g_{m1}+g_{m2})^4 |R_{out1}.R_{out2}.|^2}\right] {C_{in}}^2 {R_{in}}^2 f^2 \quad (44)$$

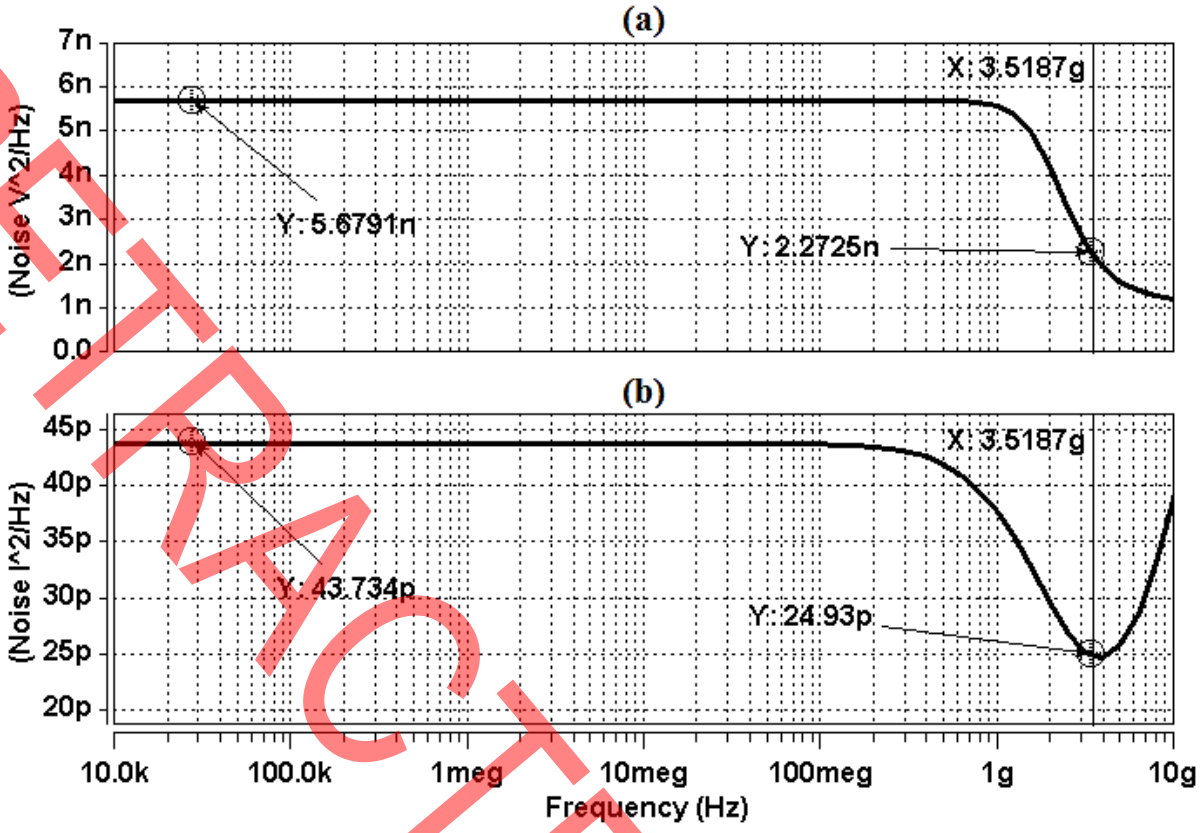


Fig 15. Output and Input referred noise of the CI-TIA

So, the value of white noise and the colored noise is specified as in (44).

As it can be concluded from equation (43) that the noise of the third stage is negligible in comparison with the noise of the first stage, so the main thermal noise for the TIA is produced in the first stage.

Hence, the total input referred noise of the proposed cascoded-inverter TIA is simulated, which shows 2.052μA_{rms}@3.981GHz (32.5pA/√Hz) input referred noise. The noise is simulated over frequency and the result is shown in figure (15). As it is obvious in figure (15), the input noise value of the proposed TIA circuit at low frequencies is equal to 43.7pA/√Hz, while at -3dB frequency is reduces approximately to 24.9pA/√Hz.

Moreover, the post-layout simulation is done for the proposed CI-TIA to examine the parasitic effects in high frequencies. Figure (16) and figure (17) demonstrate the layout and a comparison between the pre- and post-layout simulations, respectively. The results do not show a considerable difference in the operating frequency, due to the fact that 3.45GHz is not that high for parasitic

behaviors in 90nm CMOS technology to ruin the performance of the TIA. But, as it can be seen, for higher frequencies, parasitic behaviors start to lessen the frequency bandwidth.

Table (4), provides a summary performance and compares the parameters of the proposed TIA circuit with other reported designs. As the main objective of this work is to obtain a low-power TIA using g_m/I_D, the power consumption value of the proposed TIA is shown to be significantly less than other reported designs. In comparison with [32], the bandwidth is 2.6 times less than that reported in [32], due to the fact that the parasitic capacitance of the photodiode in the proposed TIA is 2.5 times larger than that reported in [32]. The gain value of [32] is much higher than the proposed TIA, which results in less input referred noise. But, the proposed TIA consumes 26 times less power, which results in an overall better performance according to the FOMs, defined as follows. Moreover, in comparison with [29], 14.5 times less power consumption is achieved in cost of less bandwidth and gain. Of course, the parasitic capacitance of the photodiode in [29] is less than the proposed design. Generally speaking, the proposed TIA provides better performance according to the following defined FOMs. Also, in comparison with [15], reference [15] shows a better FOM using larger technology, but as the focus is on the power consumption of this work, the power dissipation of the proposed TIA is considerably (about 13 times) less than that reported in [15]. Also, as our design does not use passive elements (inductors) and employs smaller technologies, the occupied chip area is considerably low. Moreover, in comparison with our previous work [9], a slightly higher gain and slightly less noise is obtained in cost of less bandwidth and slightly higher power-consumption. When it comes to a comparison between this work with the one in [35], [35] presents a Regulated Cascode (RGC) structure as a TIA, while we have presented an improved inverter structure as a TIA. In terms of noise, no direct noise is added to the input node of our circuit, while M6 and M7 in [35] add direct noise into the input node, which is a main drawback. In terms of the use of the cascoded inverter, [35] used the cascoded inverter as the booster amplifier in a RGC structure to reduce the input resistance, whose operating point is limited, and resulted in limited dynamic range according to the vertical opening of the eye-diagram. So, its application is limited. However, in order to provide a fair comparison, two Figure of Merits (FOMs) [30] are defined in table (4), as follows:

$$FOM1 = \frac{Gain \times B.W.}{P_{DC}} \left(\frac{\Omega.GHz}{mW}\right) \quad (45)$$

$$FOM2 = \frac{B.W.[GHz] \times Gain[\Omega] \times C_{in}[pF]}{In.Ref.Noise\left[\left(\frac{pA}{\sqrt{Hz}}\right)\right] \times P[mW]} \quad (6)$$

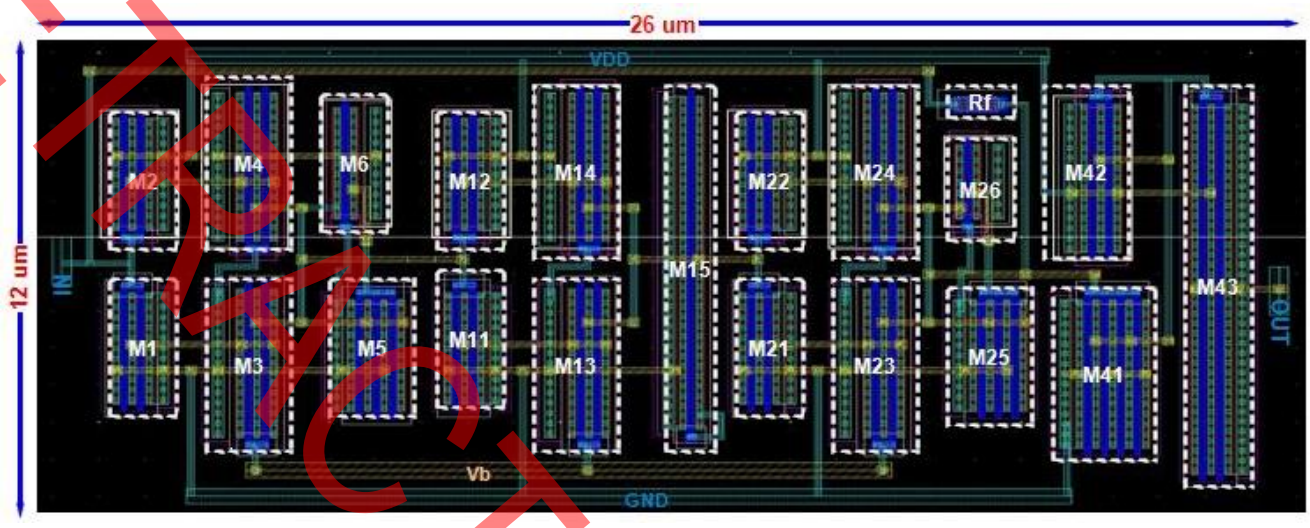


Fig 16. Layout of the proposed CI-TIA

Table 4 Performance summary and comparison with other reported designs

	[5]	[34]	[15]	[28]	[29]	[31]	[32]	[9]	This Work
Technology (CMOS)	0.35µm	90	0.18µm	0.18µm	0.13µm	0.18µm	0.35µm BiCMOS	90nm	90nm
Gain(dBΩ)	54.2	41	58	46	54	55	57.9	41	42.3
Bandwidth (GHz)	2.3	3.3	8.1	8	11.5	8.1	9	6.5	3.47
Data rate (Gb/s)	3.125	5	10	4.25	10	10	10	10	5
Power Consumption (W)	58m	5.8	34.8m	31.5m	45m	39.2m	71m	1.67	2.7m
C_{pd} (fF)	500	250	300	250	-	200	100	250	250
Supply Voltage (V)	3.3	1	1.8	1.8	1.5	1.8	3.3	1	1
Input referred noise(pA/√Hz)	18.8	14.47	15	40	6.8	16.1	11.1	33.4	32.5
No. of passive inductors	0	-	2	2	2	0	0	0	0
FoM1	20	63	184.8	50.6	128	128	98.7	436	167
FoM2	0.53	1.09	3.69	0.31	-	1.6	0.89	3.25	1.3

Chip area	465 × 435 μm^2	-	-	0.7× 0.5 mm^2	0.048 mm^2	-	-	-	26 × 12 μm^2
Implementation	Fabricated	Simulated	Simulated	Fabricated	Fabricated	Simulated	Simulated	Simulated	Simulated

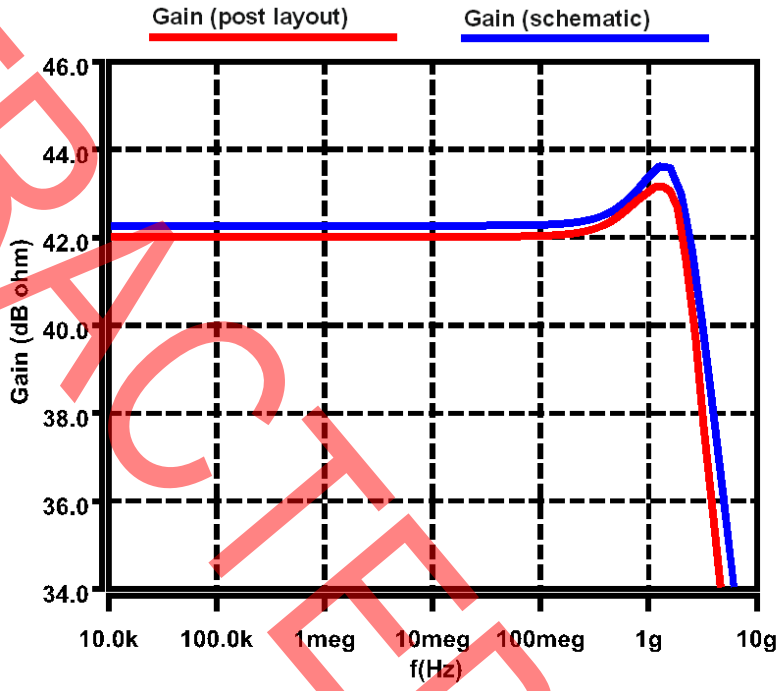


Fig 17. Comparison of pre- and post-layout simulation

6- Conclusions

A cascoded-inverter-based TIA for low-power applications is proposed in this paper, which employs g_m/I_D technique to determine the transistor dimensions and benefits from the lack of Miller capacitances in comparison with the conventional inverters. So, three stages of a cascoded-inverter-based structure are used as a TIA for optical communication systems employing active type of inductors to obtain wide bandwidth, while, occupies a small chip area in comparison with using passive inductors. Hence, poles are moved to higher frequencies and a 5Gb/s data rate is achieved consuming less power. Simulation results indicate that the proposed TIA operates suitably as a low-power, 5Gbps optical communication receiver system.

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