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CNTFET Based Pseudo Ternary Adder Design and Simulation

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ABSTRACT: Utilizing multiple logic instead of binary logic levels makes the same system to be realized with reduced number of internal connections and wiring, and occupying smaller chip area while achieving higher operational speed. In spite of all the mentioned advantages, the multilevel logic systems relay on voltage dividing mechanism to provide suitable mid-voltage outputs. However, this requires a direct current flow from supply voltage to the ground, making the structure power hungry. Eliminating the mid-voltage outputs can help the structure to resemble binary design approach and be more power efficient, as will be discussed. In this paper, pseudo ternary addition blocks, namely a Half-Adder, a Full-Adder block are designed and implemented based on CNTFET, which try to eliminate 1 output for mid-stages wherever possible. The proposed adders are implemented, simulated and verified in HSPICE software using 32nm CNTFET technology. The simulation results reveal the proposed pseudo ternary Full-Adder block consumes just 1.037 μ W power and has the propagation delay of 290 ps.

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1- Introduction

In spite of the inherent potential of multilevel logic systems provided by their variety of choices during design procedure, they have previously been practically unaffordable or even totally unattainable. Hence, the main research and implementation approach were mostly aimed toward utilizing binary (i.e. on/off based) logic systems. Recently, Carbon Nanotubes Field effect transistors have been introduced, which have made the old dream of realizing multilevel logic systems feasible. The main reason behind the simply achievable implementation of multilevel circuits based on Carbon Nanotube transistors is the possibility of changing the channel threshold voltage, V_{th}, of these transistors just by adjusting the number of their nanotubes.

CMOS technology is the predominant technology that provides scaling of the dimensions required to implement highly compact integrated circuits with a higher performance, lower power consumption, and higher density. With the inevitable reduction in the specific size of MOSFET transistors at the nanoscale, CMOS technology has faced fundamental problems and challenges.

Problems such as short channel effects, high leakage currents, high power consumption density, high sensitivity to process changes, reduced gate control, and very large channel length modulation parameter that will disrupt the process of reducing dimensions and degrading the performance of CMOS technology.

Hence, extensive research has been done in the field of electronic components in order to find alternative nanoparticles to solve these problems. These Carbon Nanotube field effect transistors could be considered as a replacement for MOSFET devices in the near future. [1, 2]

With the development of digital circuits, the length and complexity of internal connections as well as the chip level required to implement these circuits have increased. On the other hand, embedding multiple systems in a single integrated circuit will increase power consumption and reduce data processing speed [3, 4].

Achieving a way that improves the complexity of internal connections without compromising power and speed parameters is essential. Multi-level circuits are designed by increasing the number of levels of logical values from two levels (r = 2), to more than two levels (r> 2). Increasing the levels of logical values leads to a reduction in the length and complexity of internal connections. This reduction in the number of internal connections is such that M reduces the connection in binary mode to the inverse log2 M connection in multi-value mode [5]. Despite significant features such as increasing speed and reducing the volume and power consumption of the circuit, multiple logic has been less used

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by logic circuit designers due to the problems it creates in implementation [5-11].

However, new technologies introduced in the recent years, such as Carbon Nanotube Transistors (CNTFETs) and Single-Electron Transistors (SETs), have made it easier for designers to pay attention to this logic by facilitating the implementation of this type of circuit, and solving some of their problems. In addition, the use of these technologies provides better performance for logic circuits compared to silicon transistors [7, 12, 13].

In the paper [14], the 2-trit arithmetic logic unit design is presented, using CNTFETs and Resistive Random Access Memory (RRAM) as design elements. This ALU incorporates a transmission gate block, a function select block, and various ternary function processing modules. The ALU design optimization is achieved by introducing a controlled ternary adder–subtractor module instead of separate adder and subtractor circuits. In the paper [15], a serial ternary Full Adder using Carbon Nanotube technology is presented. This structure includes a ternary Full Adder and a flip-flop. The technique used to implement the circuits is to adjust the threshold voltage of the transistors. In another paper [16], the structure of the quinary (5-level logic) NAND, NOR gates and Adder are presented. A graphene nano-strip transistor with 15-nanometer transistor technology is used to implement the circuits. The simulation results in this paper show that the PDP index of quinary Adder is 179.3 fj with a supply voltage of 0.8 Volt and maximum frequency of inputs is 100 MHz.

The paper is organized as follows: In the section 2, the physical structure of CNTFET is briefly reviewed. In section 3, the conceptual circuitry and the CNTFET transistor level realization of two different three-level adders based on CNTFET technology are presented. In this section the CNTFET based pseudo ternary Full-Adder and Half-Adder are explained in detail. The simulation results are provided in section 4 and section 5 concludes the paper.

2- Carbone Nanotube Transistor

Carbon Nanotubes are composed of graphite sheets tubed inside concentric cylinders with nanometer diameter and micro-meter length. Carbon Nanotubes are divided into Single-Walled Nanotubes (SWNT) and Multi-Walled Nanotubes (MWNT) based on their number of layers. Single-Walled Carbon Nanotubes are the result of the complexity of a single layer of graphite, while multi-walled Carbon Nanotubes are the result of the complexity of several layers of nested graphite [2, 14]. The properties of nanotubes depend on their structure and act as metal or semiconductor depending on the chirality. The second characteristic of nanotubes that is affected by their electrical properties is the number of walls. The main difference between single-walled and multi-walled is the diameter of the nanotubes [18].

The arrangement of carbon atoms along the tube defines the chiral vector, and is denoted by a correct pair (n_1, n_2). Based on the chiral vector, CNT can be conductive or semiconductor. If $n_1=n_2$ or $n_1-n_2=3i$, the nanotube is metal, otherwise it is a semiconductor.

The diameter of CNT has a key role in the electrical characteristics of the transistor. The equation of the diameter CNT is:

$$D_{cnt} = \frac{\sqrt{3}\, a_0 \sqrt{n_1^2 + n_2^2 + n_1 n_2}}{\pi} \quad (1)$$

where a_0=0.142 nm , $\pi = 3.14$, and n_1,n_2 are chirality vector.

In the structure of CNTFET components, one or more non-doped semiconductor SWCNTs are used as semiconductor channel material instead of silicon bulk in the MOSFET structure [14].

The use of single-walled semiconductor Carbon Nanotubes as a substitute for silicon channel field-effect transistors has major advantages, such as lower electron scattering, higher thermal conductivity, very high electrical conductivity, and high tensile strength.

Therefore, Carbon Nanotube circuits have much less latency than silicon circuits [1,19,20]. Additionally, a CNT transistor, like a MOSFET, has a threshold voltage that is actually needed to turn on the transistor through the electrostatic gate. A very important advantage of CNTFET is that its threshold voltage can be adjusted by changing the diameter of the Carbon Nanotubes.

This practical feature makes CNTFETs much more flexible for designing digital circuits than MOSFETs, and makes the technology very suitable for designing multi-voltage threshold circuits.

The threshold voltage of a CNTFET can be calculated by Equation 2:

$$V_{th} \cong \frac{E_g}{2.e} = \frac{\sqrt{3}}{3} \frac{a.V_\pi}{e.D_{CNT}} \cong \frac{0.43}{D_{CNT}\left(nm\right)} \quad (2)$$

Here a is the atomic distance of carbon to carbon, Vp is the π–π junction energy of Carbon, e is the electrical charge unit, and DCNT is the diameter of Nano-tube Carbon.

This diameter can be calculated by the following equation in which the CNTFET threshold voltage is an inverse function of the CNT diameter:

$$D_{CNT} = \frac{C_h}{\pi} = \frac{a\sqrt{n_1{}^2 + n_2{}^2 + n_1 n_2}}{\pi} = 0.0783\sqrt{n_1{}^2 + n_2{}^2 + n_1 n_2} \quad (3)$$

A Carbon Nanotube transistor looks like a MOSFET with the same pins. In other words, the principles of operation of Carbon Nanotube field effect transistors are similar to current

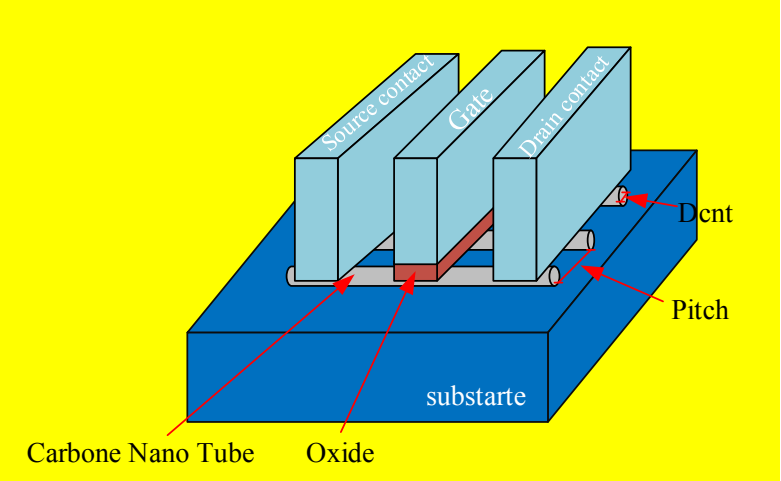


Fig. 1. The structure of CNTFET [14]

silicon transistors. Figure (1) shows the physical appearance of a Carbon Nanotube transistor [14]. The nanotube remains no doped in the area below the gate.

The two ends of the nanotube that connect to the source and drain connections are doped areas. The voltage applied to the gate of the transistor can control the electrical conductivity of the Carbon Nanotube in the area below the gate by changing the electron density in the channel.

The distance between the cross-sectional centers of two adjacent Carbon Nanotubes below the transistor gate is called a "pitch", which significantly affects the width of the gate and the drain, and source of the transistor. Interestingly, the PCNTFET and NCNTFET have the same current rate.

The gate width of the transistor can be estimated based on equation (4), in which N is the number of nanotubes under the gate, D_{CNT} is the diameter of the nanotube, and W_{min} is the minimum possible width for the gate, which is determined based on lithographic constraints.

$$W_{gate} \approx Max\,(W_{\min}, (N-1)pitch + D_{CNT}) \qquad (4)$$

3- Arithmetic Pseudo Ternary Blocks

As mentioned earlier in the paper, due to noticeable capabilities of multi-level systems and its feasibility utilizing Carbon Nanotube transistors, Half-Adder, and Full-Adder blocks are implemented based on a three-value (i.e. ternary, basis).

The circuits design procedure of these blocks are described at the following sections.

3- 1- Inverting Ternary Block

One of the most essential blocks in the design of three-level ternary circuits is an inverting block. The ternary base includes three meaningful logic levels. These logic levels can be represented by symbols "0", "1", and "2", which are usually equivalent to the voltage levels 0, (VDD/2), and VDD, respectively. In general, a three-value inverter, with input "*a*" and output *Not (a)*, is expressed by equation (5) and has three definable types.

$$NOT_i(a) = \begin{cases} i & \text{if} \quad a=1 \\ 2-a & \text{if} \quad a \neq 1 \end{cases} \qquad (5)$$

By selecting the ternary logic values "0", "1", and "2" for "*i*" in equation 6, a three-value inverter can be a Negative Turning Inverter (NTI), a Standard Turning Inverter (STI) and a Positive Turning Inverter (PTI). Based on equation (5), the truth table of these three types of inverters are in the form of Table 1 [21].

The NTI and PTI circuits are shown in Figure 2. Each inverter consists of an N-type Transistor (i.e. NCNTFET), and a P-type Transistor (i.e. PCNTFET transistor). The number of nanotubes differs for NTI and PTI inverters. In NTI configuration for inputs equal to 1 and 2, the NCNTFET must be turned on to make the output node 0, hence the threshold voltage of NCNTFET must be less than 0.45volt. This can be achieved by selecting the number of NCNTFET nanotubes N equal to 19 to set the NCNTFET threshold voltage at 0.3. On the other hand, in PTI configurations it is vice versa, and hence the number of PCNTFET nanotubes N is selected as 19 to set the PCNTFET threshold voltage at 0.3. In this case, for inputs 0 and 1 the output becomes 2. In both cases, for other transistor N is selected 10 (Refer to Fig. 2). A_barn and B_barn are the outputs of NTI_A and NTI_B inverters with inputs A and B, respectively. In addition, A_barp and B_barp are the outputs of PTI_A and PTI_B inverters with inputs A and B, respectively.

Table 1. The truth table of ternary inverters

Input(a)	NTI (a)	STI (a)	PTI (a)
0	2	2	2
1	0	1	2
2	0	0	0

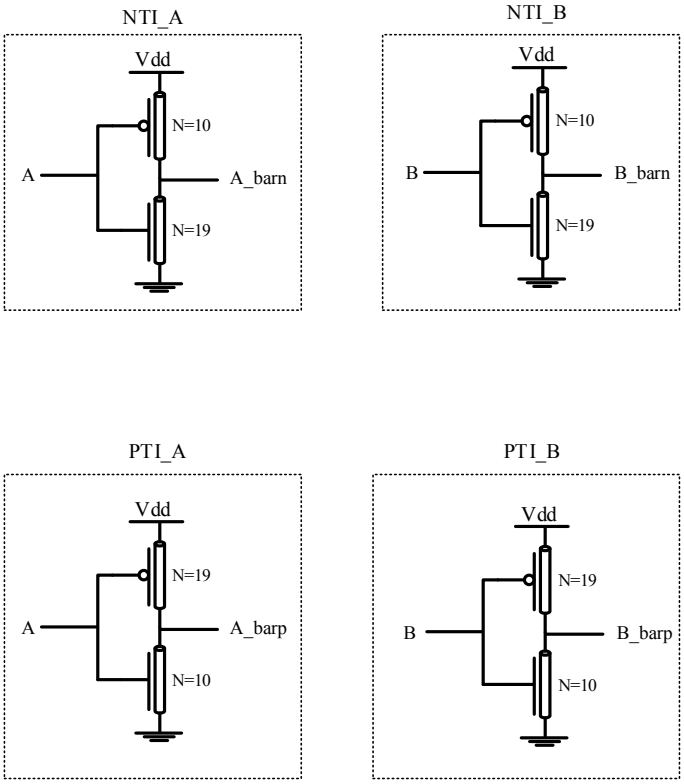


Fig. 2. Inverting Ternary circuit realization

3- 2- The Proposed Pseudo Ternary Half-Adder

Half-Adder is the most basic addition block which is used almost in every arithmetic operation. Half-Adder has two inputs namely A and B, and usually generates two outputs (i.e. Sum and Carry). However, considering three definable types for three-value based blocks, for proposed pseudo ternary Half-Adder, the outputs Sum, Carry and Carry_bar are generated for which further explanations will be provided later in the paper. Tables 2 and 3 shows the proposed pseudo ternary Half-Adder outputs, Sum, Carry and Carry_bar, for the inputs A and B.

As mentioned earlier, considering a unique methodology to generate the output node ternary logic is essential for a successful and efficient design procedure.

Ternary Logic Design methodology to create desired Output value:

To create logic 2, a path of transistors is required to connect the VDD supply voltage to the output node. Considering that the logic value 2 or VDD Voltage can be easily transferred using P-type topologies, P-type CNTFET transistors will be adopted in this case.

To create logic 1, both P-type and N-type topologies must be utilized at simultaneously on condition, acting as a voltage divider. Remember that for middle stages logic 1 is eliminated for pseudo ternary architectures to optimize the power consumption scheme.

To create logic 0, a path of transistors is required to connect the GND voltage to the output node and in this case N-type transistors will be used to create a zero level in the output.

Note that the half adder has not any middle stages but necessary precautions must be take into account to use it

Table 2. Look up table of the Sum output of the proposed pseudo ternary Half-Adder

A	B	Sum
0	0	0
0	1	1
0	2	2
1	0	1
1	1	2
1	2	0
2	0	2
2	1	0
2	2	1

successfully to build a Pseudo ternary full adder as will be discussed in next session.

3- 2- 1- The Sum Output of the Proposed Pseudo Ternary Half-Adder

Table 2 shows the look up table of the Sum output of the pseudo ternary Half-Adder for all possible cases of its two ternary weighted inputs (i.e. A and B). In the following paragraphs, the implementation tips of the Half-Adder Sum output will be explained.

Considering the Sum output of the Half-Adder truth table (refer to Table. 2), for A equal with 0, the exact value of B appears in the Sum output, and for B equal with 0, the exact value of A appears in the Sum output. The best solution to realize these cases with minimum number of transistors is to utilize the pass transistor topology in which both the gate and the source terminal of the transistor are considered as inputs (Consider Structure 1 at Figure 3).

Hence Structure 1 provides the correct outputs for AB=00, AB=10, AB=01, AB=20, and AB=02 input cases. A_barp input in Structure1 of Figure 3 is shown at Figure 2.

When the inputs are AB=11, the Sum output is 2, and as a result, the P-type structure can be used to create Sum output of 2.

As shown in Figure 3, structure 2 aims to connect the output node to supply voltage Vdd for inputs A=1 and B=1. Hence, it includes two series PTI PCNTFET transistors with N=16 to create output 2. Since structure 2 must be open for inputs A=0, B=1 and A=1, B=0, another two series PCNTFET transistor are included with A_barn and B_barn inputs to ensure output 2 just for the case A=B=1. NTI inverters utilized to create A_barn and B_barn at their input are as described in Figure 2.

For inputs A=1, B=2 and A=2, B=1, the sum output must be zero. In this case, the transistors in structures 3 and 4 are used to create the correct output. In these structures, NCNTFET transistors can be easily turned on while their gate inputs are 2, but for the case where their gate input is 1, the number of transistors nanotubes (i.e. N) and hence their threshold voltage must be adjusted that they can be turned on for input 1 (i.e. voltage Vdd/2). That is why the size of transistors are different for structure 3 and 4 in figure 3. In order to eliminate connection to ground for A=2 and B=2, another PTI NCNTFET transistor is added in series. The NPI inverters embedded at the input of each of them are as described at Figure 2.

Considering Figure 3 for a clear explanation, suppose that for A=2 and B=1, structure 3 must make the output zero. For this purpose, three transistors with A, B, and B_barp gates are connected in series.

The reason behind using the third transistor is that, if the NCNTFET transistor B is connected to its gate equal to 1, it will be also connected to input 2. Meaning that in the absence of the B_barp transistor, structure 3 makes the output 0 for A=2, B=1 and A=2, B=2. To prevent this, we use a third transistor, the gate of which is controlled by B_barp, so that the output does not connect to ground if A=2 and B=2.

For the case of AB=12, the same conditions should be considered. To create output 1, structure 5 is used, which is used to create this logic at the output of network N and P, simultaneously.

3- 2- 2- The Carry and Carry_bar Output of the Proposed Pseudo Ternary Half-Adder

Referring to the Carry output of the Half-Adder truth table at Table. 3, it is obviously seen that it never becomes 2 for all possible input cases. As previously declared, pseudo ternary design approach aims to eliminate logic value 1 at mid-stage output nodes. Considering that a full adder consists of two cascaded half adders, and that the half adder carry never becomes 2, which encourages the pseudo ternary design approach as will be described in the following sections.

As will be shown, generating complement of Carry output (i.e. Carry_bar) given at Table. 3 in which the logic value

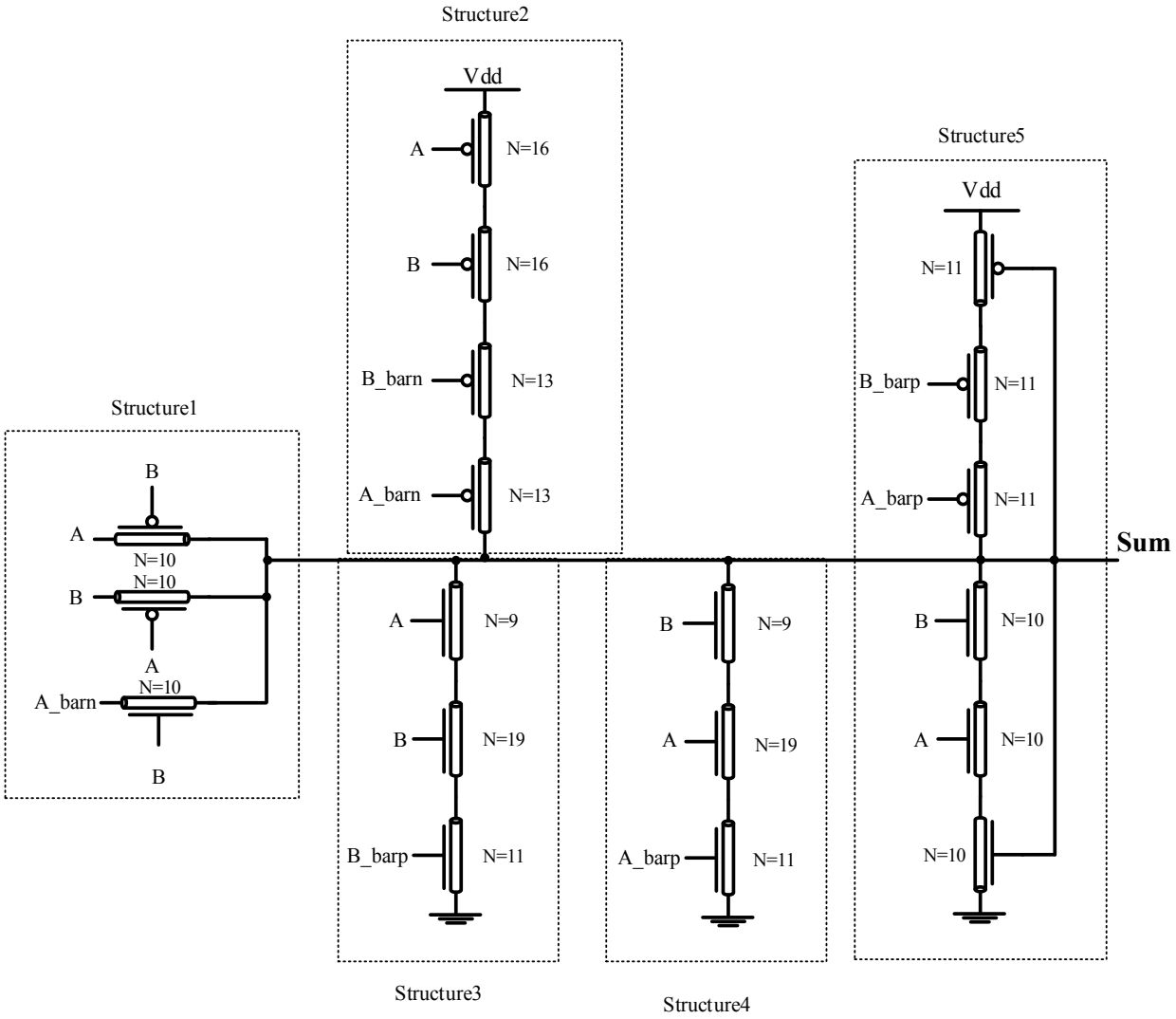


Fig. 3. The CNTFET transistor level realization of Sum output of the proposed ternary Half-Adder

Table 3. Truth table of the proposed ternary Half-Adder Carry output

A	B	Carry	Carry_bar
0	0	0	2
0	1	0	2
0	2	0	2
1	0	0	2
1	1	0	2
1	2	1	0
2	0	0	2
2	1	1	0
2	2	1	0

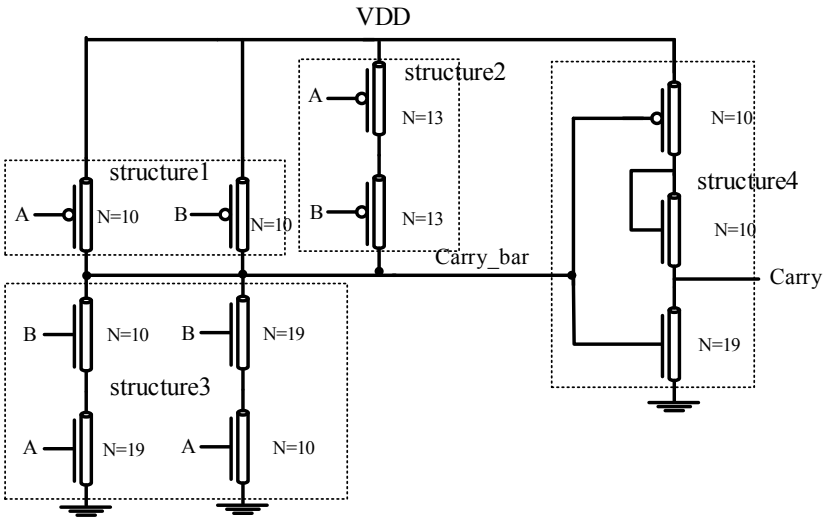


Fig. 4. The CNTFET transistor level realization of Carry output of the proposed pseudo ternary Half-Adder

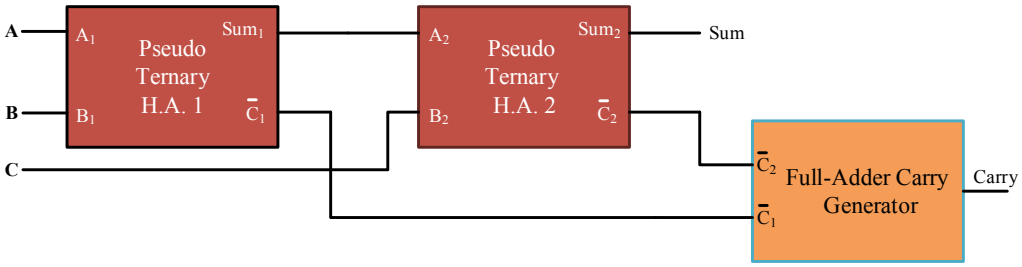


Fig. 5. The block diagram of the proposed pseudo ternary Full-Adder

1 eliminated, matches well with the full adder design. For general purpose designs, an inverter is included after Carry_bar output (Structure 4 of Figure. 4) to generate Carry output (which in the proposed circuit it is not necessary in this paper).

The CNTFET transistor level realization of Carry_bar and Carry output of the proposed pseudo ternary Half-Adder is depicted in Figure 4.

According to the truth table of Table. 3, for A=0 and/or B=0 (five out of nine cases), the Carry_bar output must be 2. This is guaranteed by two parallel PCNTFET transistors (Structure 1 of Figure. 4) which connects Carry_bar to Vdd.

For A=B=1, the Carry_bar output is also 2 which can be realized utilizing two series PCNTFET transistors (Structure 2 of Figure. 4) to connect Carry_bar to Vdd. Also note that for either inputs A or B equal to 0, this structure connects Carry_bar to Vdd which according to the truth table is correct.

For cases 5, 8 and 9 (AB=12, 21 and 22, respectively), the Carry_bar output must be 0. Structure 3 of Figure. 4, including two parallel branch of series NCNTFET transistors, guarantees the Carry_bar output to be connected to ground.

Structure 4 of Figure. 4 is embedded to convert Carry_bar output to Carry. This structure connects the Carry output to ground when Carry_bar is 2, and makes the Carry equal to Vdd when Carry_bar is 0. In order to do this, a diode connected NCNTFET transistor is placed in the pull up network between Carry and Vdd.

3- 3- The Proposed Pseudo Ternary Full-Adder

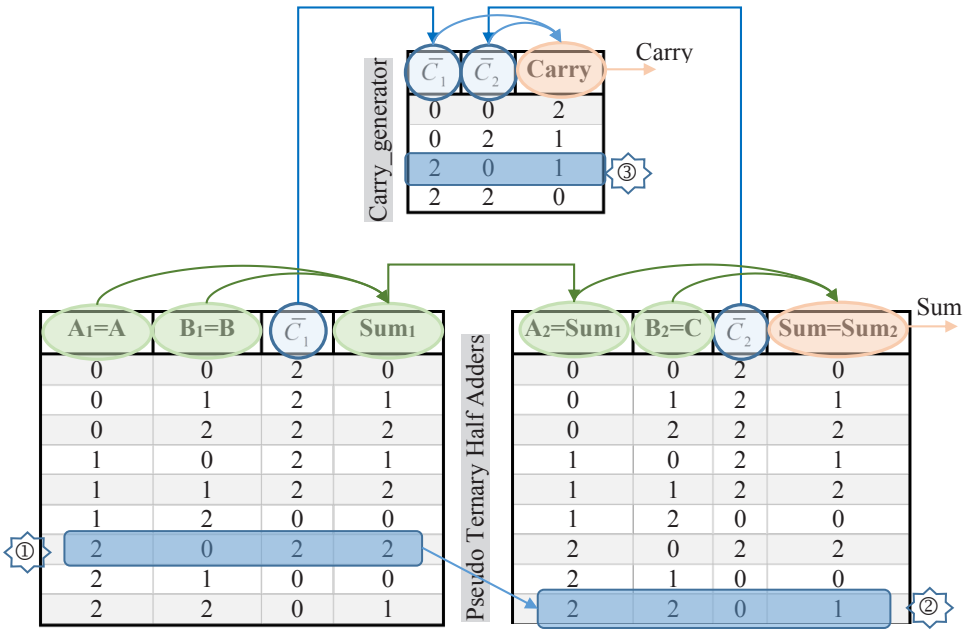
The proposed pseudo ternary Full-Adder consists of two pseudo ternary half adder and a Carry Generator, as shown in Figure 5. It is used to sum three ternary digits. These blocks accept three inputs namely A, B and C, and generate two outputs, Sum and Carry. Table 4 shows the proposed ternary Full-Adder Carry, Carry_bar and Sum outputs, considering three inputs A, B and C.

The complement carry empowered pseudo ternary half adder based Full Adder benefits a power consumption efficient design, utilizing a pseudo ternary configuration in which the occurrence of 1 outputs at carry outputs are eliminated in middle stages. In other words, the Carry_bars of the half adders are utilized along with the carry generator. The truth table of this carry generator is given by Table. 5.

Table 4. Truth table of the proposed conventional ternary Full-adder outputs

No	A	B	C	Carry	Sum
0	0	0	0	0	0
1	0	0	1	0	1
2	0	0	2	0	2
3	0	1	0	0	1
4	0	1	1	0	2
5	0	1	2	1	0
6	0	2	0	0	2
7	0	2	1	1	0
8	0	2	2	1	1
9	1	0	0	0	1
10	1	0	1	0	2
11	1	0	2	1	0
12	1	1	0	0	2
13	1	1	1	1	0
14	1	1	2	1	1
15	1	2	0	1	0
16	1	2	1	1	1
17	1	2	2	1	2
18	2	0	0	0	2
19	2	0	1	1	0
20	2	0	2	1	1
21	2	1	0	1	0
22	2	1	1	1	1
23	2	1	2	1	2
24	2	2	0	1	1
25	2	2	1	1	2
26	2	2	2	2	0

Table 5. Truth table of the proposed pseudo ternary Full-adder outputs



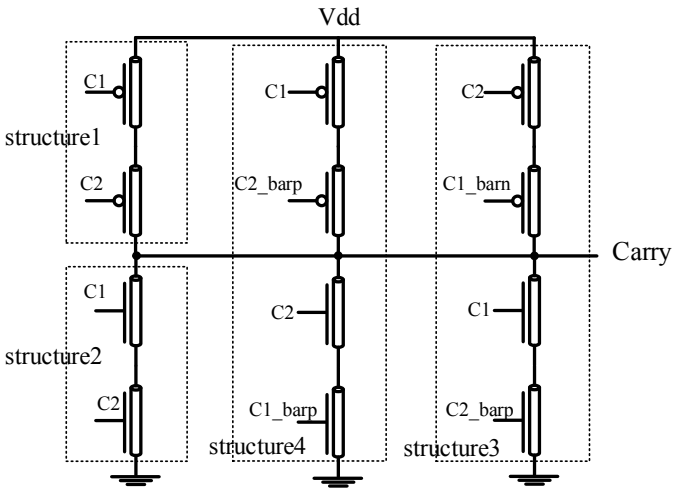


Fig. 6. The CNTFET transistor level realization of the pseudo ternary full adder Carry generator circuit

3- 3- 1- The Sum Output of Pseudo Ternary Full Adder

Sum output of the pseudo ternary full adder has a configuration similar to the binary. As mentioned earlier, the pseudo ternary modifications can be applied to the middle stages which only have two out of three ternary logic levels, including 1. Since sum output appears simultaneously at middle and last stages of the topology, and meanwhile all three ternary logic levels do exist in it, applying pseudo ternary design scheme is not possible considering either the modularity or logical points of view.

3- 3- 2- The Carry Output of Pseudo Ternary Full Adder

The proposed pseudo ternary Full-Adder Carry generator circuit is designed based on Carry_bar. The truth table to design the Carry_generator circuit is included in Table 5. In fact, if the Half-Adder Carry output is used in the circuit design, since its outputs are 0 or 1, it will not only require additional number of transistors to create output 1 implying a direct power hungry path from Vdd to ground, but also an extra inverter will be needed. Thus, it is better to use inverse of Carry output for circuit realization to simplify the circuit implementation of the Full-Adder. This technique reduces the propagation delay of the full adder while eliminating inverters.

In order to validate Table 5 versus Table 4, consider line 20 of Table 4 in which ABC = $(202)_3$ = $(3\times2^2+0\times3^1+2\times3^0)_{10}$ = $(18+2)_{10}$ = $(20)_{10}$. According to Table 5, the first selection is line 1 in which A_1=A=2, B_1=B=0, and the resulted outputs are $\overline{C}_1$=2 and Sum_1=2. Since A_2= Sum_1=2 and B_2=C=2, the second selection is line 2, and the resulted outputs are $\overline{C}_2$ =0 and Sum=Sum_2=1. In the last try, since $\overline{C}_1$=2 and $\overline{C}_2$ =0, the last selection (i.e. line 3 of Table 5) reveals Carry to be equal to 1. The achieved results (i.e. Carry=1 and Sum=1) are according to the information provided at line 20 of Table 4, and both results are validated successfully.

Due to the fact that the output of the Carry_bar digit has no more than two logic levels (i.e. 0 and 2), therefore we have four modes for Carry_generator circuit, as shown in the table 5. This makes the transistor level implementation feasible with minimum number of transistors. The Carry output is 2 when two inputs $\overline{C}_1$ and $\overline{C}_2$ are both 0. This can be realized by two series of PCNTFET transistors at pull up block of structure 1, as shown in Figure 6. The Carry output is 0 when two inputs $\overline{C}_1$ and $\overline{C}_2$ are 2. This can be realized by two series of NCNTFET transistors at pull down block of structure 2, as shown in Figure 6. For cases when either $\overline{C}_1$ or $\overline{C}_2$ is 0 while the other is 2, the Carry output is 1. This can be realized by structure 3 and 4, as shown at Figure 6 according to the design methodologies mentioned earlier in this paper.

4- Simulation Results

To test the correct operation of the proposed arithmetic circuits, they are simulated at HSPICE software using 32 nm CNTFET transistor model. All proposed blocks have been simulated at the transistor level utilizing the power supply of 0.9 V. The results show that for all possible input cases, the outputs of the Half-Adder and Full-Adder are correct. Figure 7 shows the transient time response of the Half-Adder sum and carry outputs, considering all possible cases for inputs A and B. The power consumption and propagation delay of the Half-Adder achieved from simulation results will be 0.389 µW and 110 ps, respectively.

Figure 8 shows the transient time response of the Full-Adder sum and carry outputs, considering all possible cases for inputs A, B, and C_{in}. The power consumption and propagation delay of the Full-Adder achieved from the simulation results will be 1.037 µW and 290 ps, respectively.

The proposed design circuit was studied under the

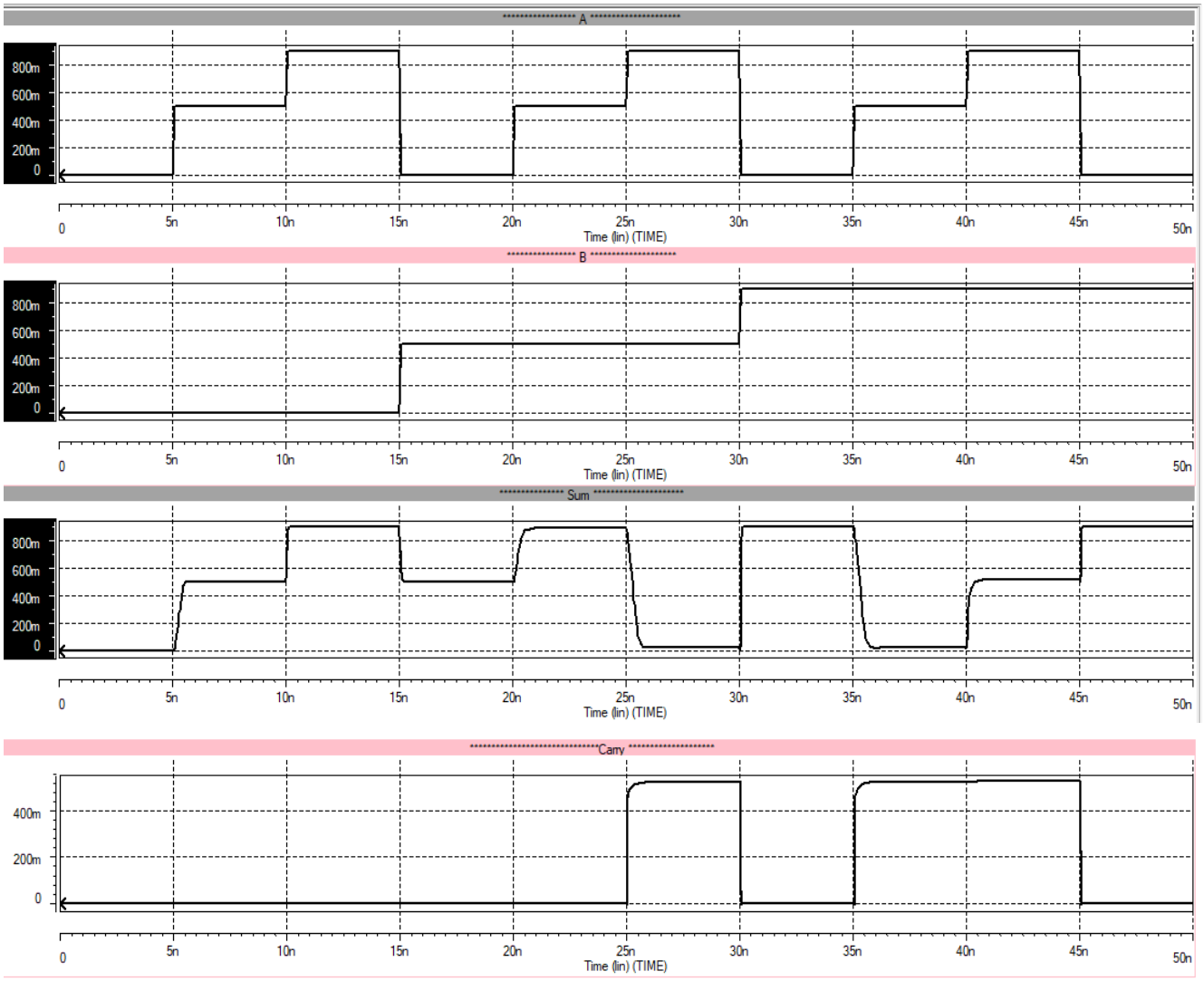


Fig. 7. The proposed ternary Half-Adder Waveform (inputs: A and B, and outputs Carry and Sum).

loads of 0.5 fF, 0.8fF, 1 fF, and 1.2fF. Figure 9 shows the power consumption of the proposed Full-Adder versus the Capacitance Loads (CL). The propagation delay of the proposed Full-Adder is shown in Figure 10. The propagation delay increases with increasing the Capacitance Load. The PDP index of the proposed Full-Adder versus Capacitance Loads is also shown in the Figure 11.

The simulation results using the Hspice software show that the power dissipation of the proposed Full-Adder increases from 0.95 µW to 1.39 µW in exchange for changing the temperature from 10 ºC to 80 ºC. The power dissipation curve versus temperature is shown in Figure 12. The propagation delay and the proposed PDP index of the proposed Full-Adder versus Temperature (ºC) are shown respectively in Figures 13 and 14.

Table 6 compares the proposed ternary blocks to some other state of the art works. The results reveal the least Power-Delay Product (PDP) index of 301 (aj) for proposed Full-Adder block. The number of transistors required to implement the proposed Full-Adder and Half-Adder are 66 and 30 transistors, respectively.

5- Conclusion

The overall performance of multilevel logic systems can distinguishably have enhanced due to the reduced number of internal connections and wiring. The novel proposed pseudo ternary multilevel logic systems on the other hand help to decrease the overall power consumption of the system by eliminating the current flow hungry paths from middle stages. Multilevel ternary logic system realization

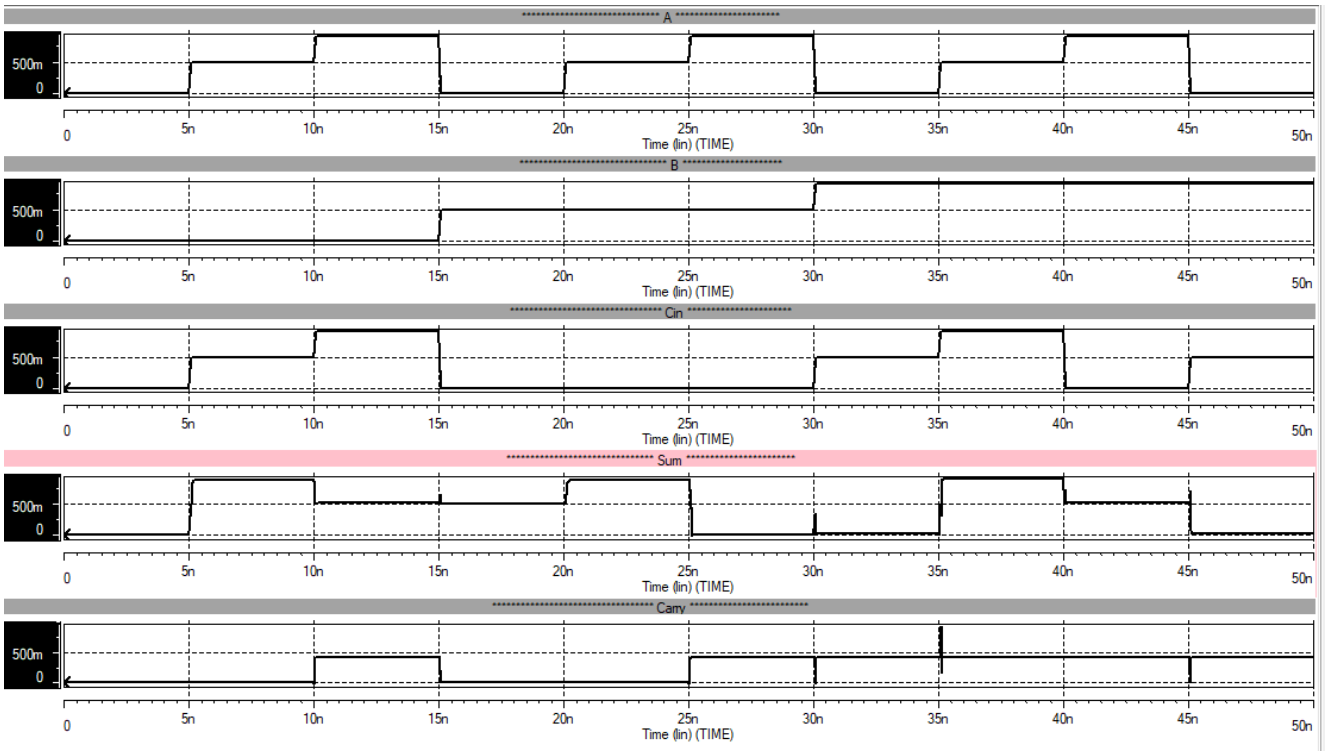


Fig. 8. The proposed ternary Full-Adder Waveform with 1fF Capacitance Load (inputs: A, B and Cin and outputs Carry and Sum).

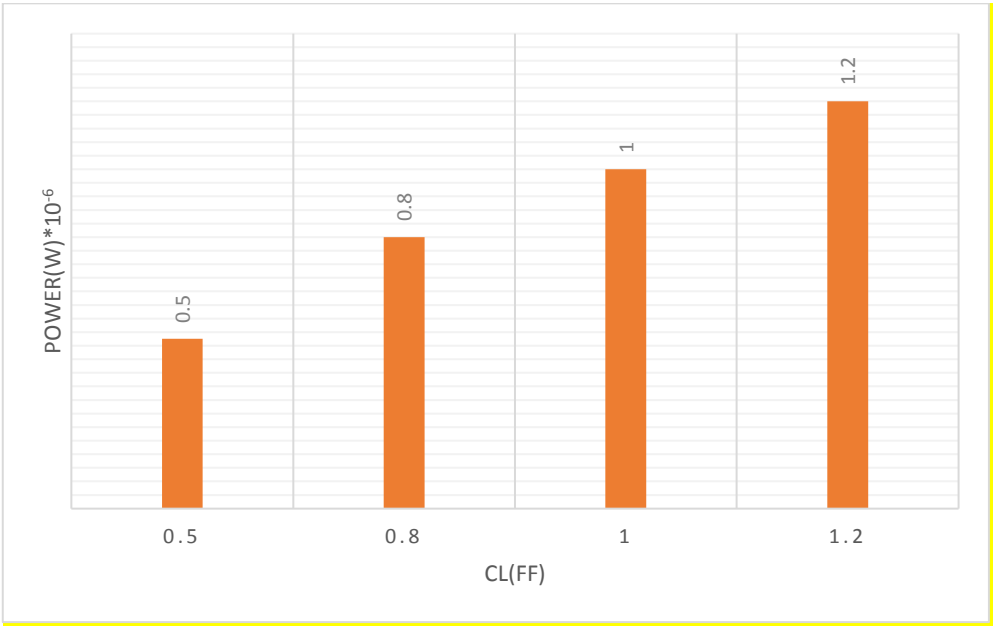


Fig. 9. The power consumption versus Capacitance Loads

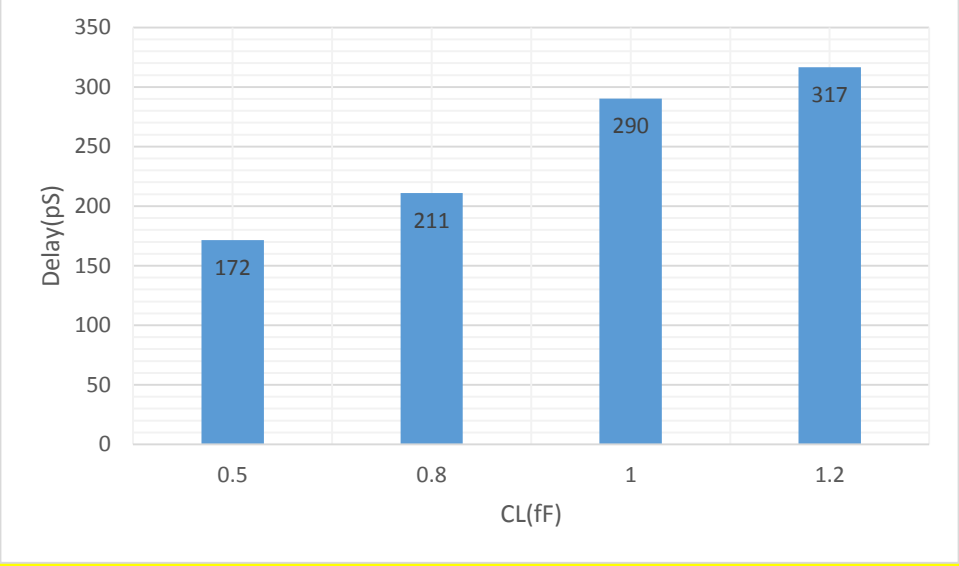


Fig. 10. The propagation delay of proposed Full-Adder versus Capacitance Loads

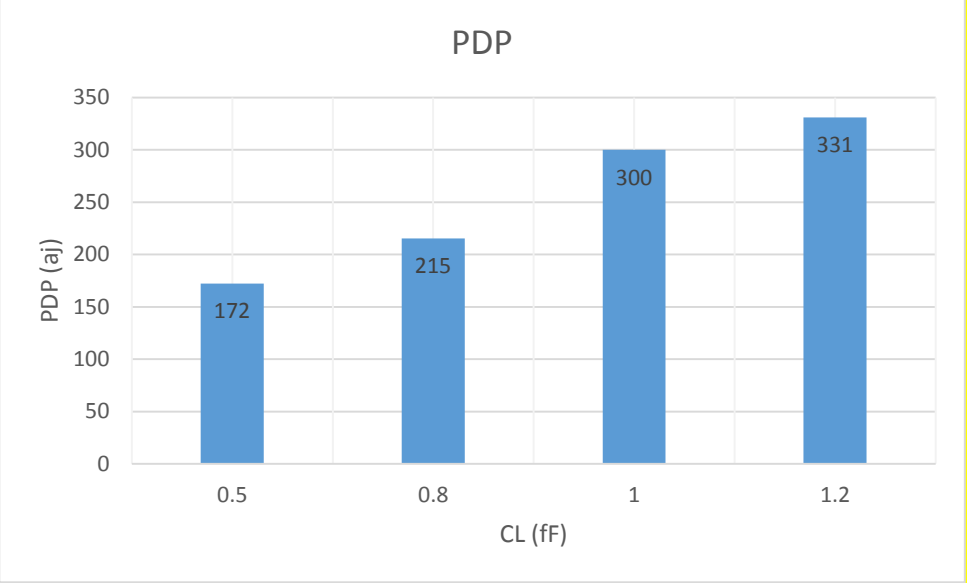


Fig. 11. The PDP value versus Capacitance Loads

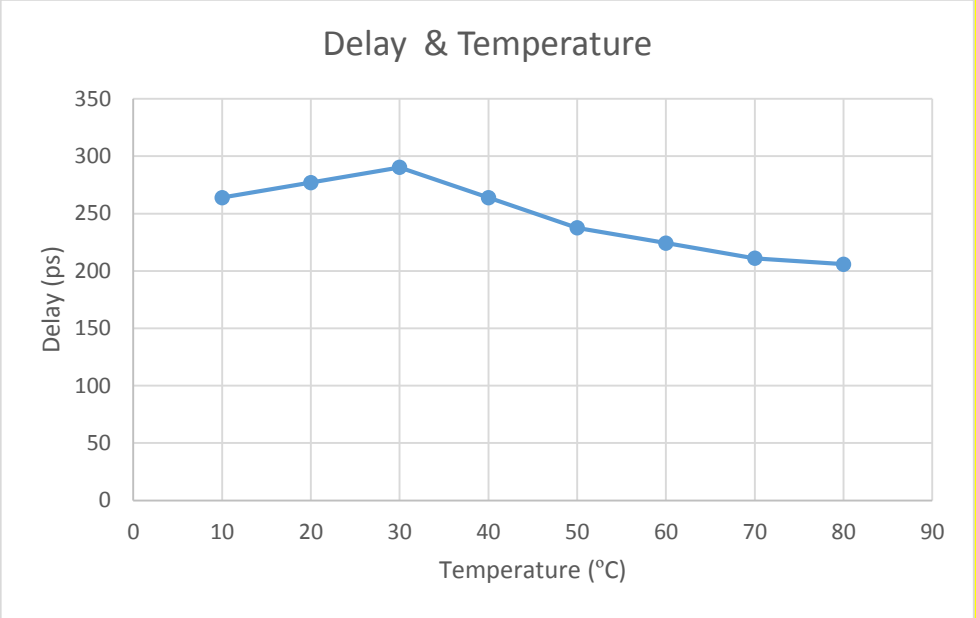


Fig. 12. The power consumption versus Temperature

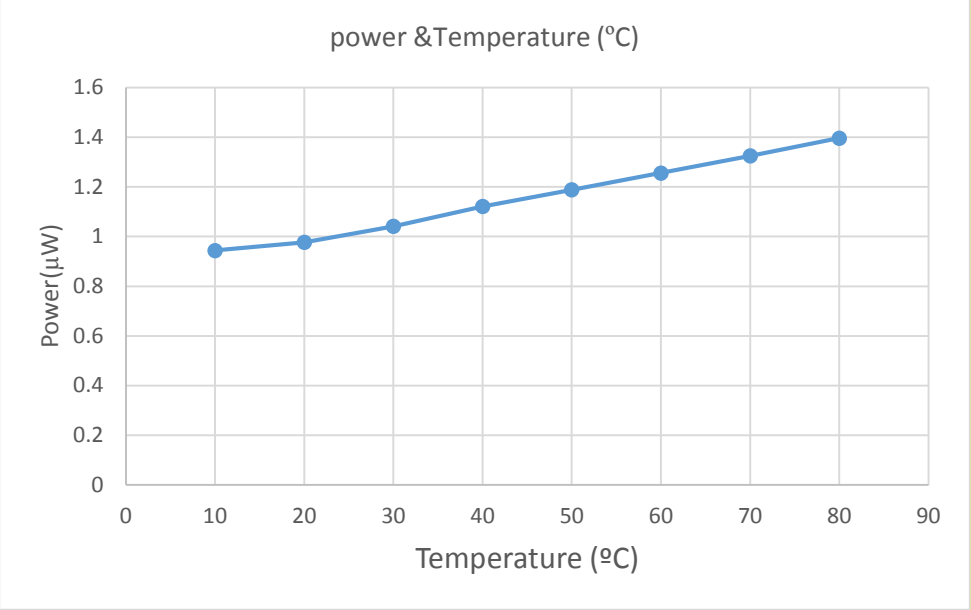


Fig. 13. The propagation delay of the proposed Full-Adder versus Temperature

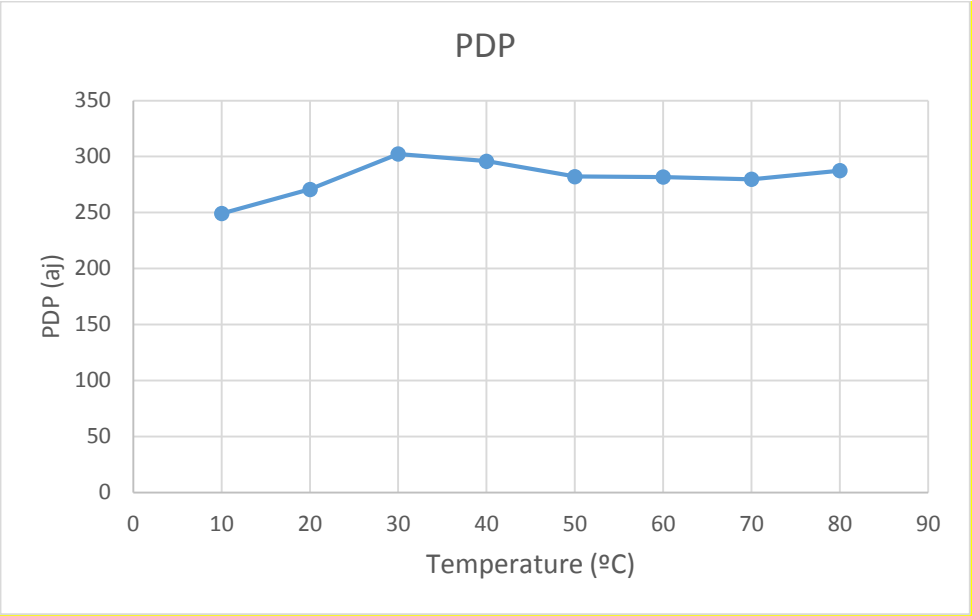


Fig. 14. The PDP index of proposed Full-Adder versus Temperature

Table 6. Comparing the proposed CNTFET based ternary weighted arithmetic blocks with other state of the art works

Structure	References	Propagation Delay Time (ps)	Consumption Power (μW)	PDP (aJ= ps × μW)
Ternary Full Adder	**Proposed**	**290**	**1.037**	**301**
	[15]	200.17	28.49	5702
	[22]	386.1	1.462	564
	[23]	22.8	14.2	323
	[12]	283.8	6.361	1805

by CNTFET has its own challenges, especially for providing voltage $V_{dd}/2$ utilizing a voltage divider. In this paper, pseudo ternary addition blocks, namely a Half-Adder and a Full-Adder blocks are designed and implemented based on Carbon Nanotubes Field effect transistors, which try to eliminate 1 output for mid-stages wherever possible. In other words, adapting a combination of binary/ternary circuit design techniques an optimized design and implementation solution has been achieved, which help the system to occupy smaller chip area while achieving higher operational speed and less power consumption.

The proposed adders are implemented, simulated and verified in HSPICE software using 32nm Carbon Nanotube transistor technology file provided by Stanford University. The simulation results reveal the proper operation of the blocks while the proposed pseudo ternary Full-Adder block consumes just 1.037 mWatt power, and has the propagation delay of 290 ps. The results reveal the Power-Delay Product (PDP) index of 301 aj for proposed Full-Adder block.

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