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An Active Pixel Sensor with Built-in a Unity Gain Buffer

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ABSTRACT: This paper presents an Active Pixel Sensor (APS) with a built-in readout circuit. A unity-gain buffer as a pixel readout circuit is used to read the signals of four adjacent pixels. Compared to the conventional four-transistor APS (4T-APS) which is connected to a CMOS source-follower readout circuit, the introduced circuit has higher accuracy, higher linearity, and fewer transistors. Due to the high linearity and accuracy of the pixel readout circuit, the proposed method can help to improve the final image quality of the sensor. For a fair comparison between the conventional 4T-APS (with source-follower readout circuit) and the proposed circuit, both circuits are designed with the same power consumption. Simulation results show that the proposed circuit is 16% more accurate, has an 11% higher fill factor, and is 10 dB more linear than the conventional circuit. The total power consumption of the proposed circuit with a built-in buffer is almost 17 µW with a 1.8 V power supply, and its layout size is 14.8µm×14.8µm. The total number of transistors used in this method to read the signals of four Pinned-Photodiodes is 11, whereas in the conventional method, 16 transistors are required under the same circumstances. The proposed circuit is designed in 0.18µm CMOS technology.

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1- Introduction

Digital Still Cameras (DSCs) are electronic devices that can convert photographs into digital data. DSCs are abundantly used in industrial, military, medical, and commercial equipment. For instance, DSCs are used in almost all smartphones today. According to the production of hundreds of millions of smartphones annually, an incredibly huge market has been created for digital cameras. Therefore, the development and improvement of these digital cameras can be a very suitable field for research [1]. Digital cameras are composed of two parts, including optical components and an image sensor. The image sensor (imager) captures photographs in digital memory. As shown in Figure 1, image sensors have different blocks such as pixels, a pixel array, a row decoder, a control unit, pixel readout circuits, and analog-to-digital converters. [2-4].

A pixel array is composed of many pixels in rows and columns which convert the incident light of different spots of a photograph into analog signals [5-6]. To generate a color image, different pixels of the array can be made sensitive to three basic colors of red, green, and blue (RGB code) using a Bayer filter. In fact, by putting a color filter on the pixel, the lighting color code of that spot can be measured. The pattern of the Bayer filter is shown in Figure 2 [7]. In this paper, a new combination of pixels and pixel readout circuit is proposed. Using this new method, not only the silicon area of the sensor can be reduced, but also the photo-detector signal can be read with higher linearity and accuracy compared to using the conventional one.

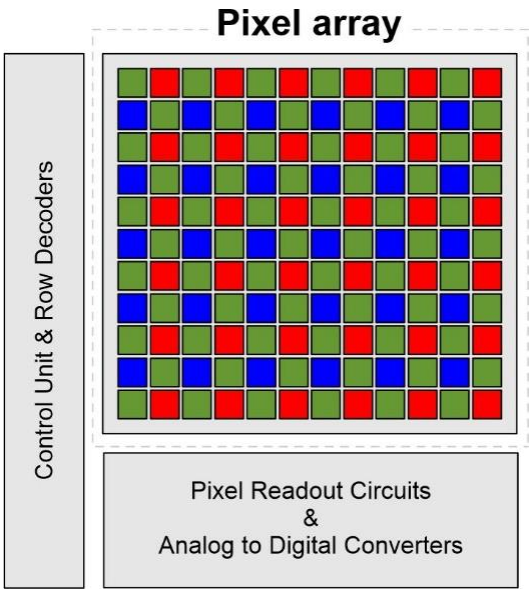

Fig. 1. Block diagram of an image sensor

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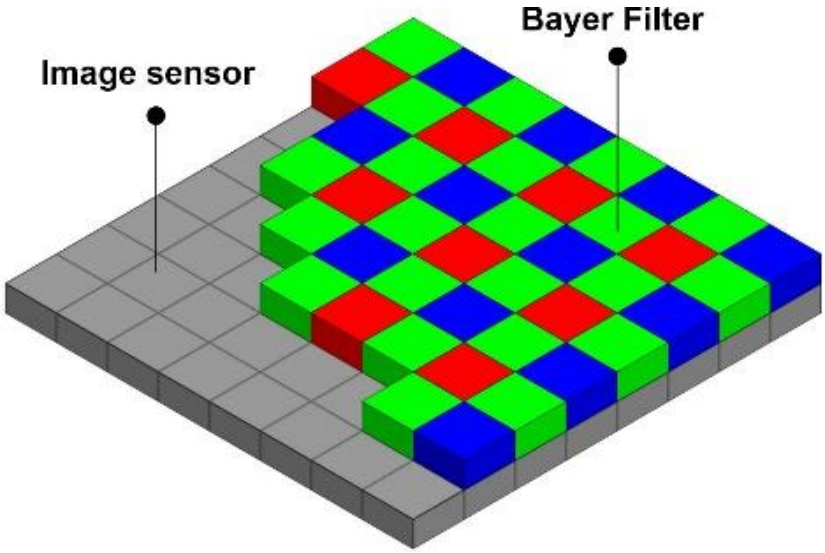

Fig. 2. The Bayer arrangement of color filters on the pixel array

In the following, the paper is organized as follows. Section 2 presents a brief overview of CMOS Image Sensors. Section 3 describes the proposed method. In Section 4, the performance and simulation results are shown. Finally, the conclusions are presented in Section 5.

2- CMOS Image Sensor

Both Charge-Coupled Devices (CCDs) and CMOS Image Sensors (CISs) are used to manufacture digital cameras. However, CMOS technology is growing at an astonishing rate while CCD is almost obsolete. The rapid growth of CMOS technology has made it possible to produce sensors with a resolution of hundreds of megapixels with high accuracy and speed. Due to the use of CMOS technology in image sensors, it is possible to not only implement photodetectors, amplifiers, and analog to digital converters, but also to implement memory and digital decoders inside the chip.

2- 1- Pixels

One of the most important parts of image sensors are the pixels. Pixels are responsible to convert light to analog signals. By measuring these analog signals, the light intensity that is focused on the pixel can be obtained. The light intensity of various spots of a 2-dimensional image can be measured by a sensor that has an abundant number of pixels in rows and columns. Photodiodes are normally used as photodetectors to design pixels. Nowadays, Pinned-Photodiodes (PPD) are more common due to low noise and low dark current. The structure of this type of photodetector is shown in Figure 3.

A Pinned-Photodiode is different from a PN photodiode in way that an extra layer of p+ with high doping is created on its surface and makes a PNP structure. The n region is completely free of charge and has potential. Compared to normal photodiodes, a Pinned-Photodiode decreases dark current and noise due to lower stimulation of electrons bu having a layer containing high doping of holes [8].

2- 2- Pixel Readout Circuit

By applying light to the surface of the photodiode, the reverse current is changed and affected by light intensity. By measuring the reverse current, the light intensity can be easily calculated. There are different types of circuits to bias photodiodes among which three-transistor APS (3T-APS) and four-transistor APS (4T-APS) are the most common types. A photodiode and a Pinned-Photodiode are used as photodetectors in the structure of 3T-APS and 4T-APS, respectively. Nowadays, a 4T-APS structure is used to design pixels, and its schematic is shown in Figure 4 [9].

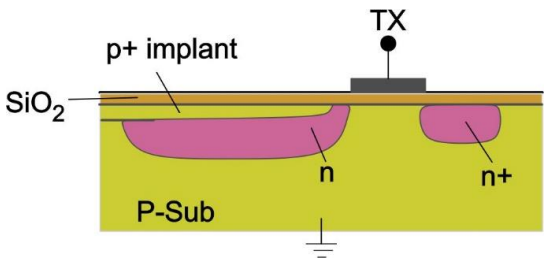

Fig. 3. Cross-section of a typical pinned photodiode

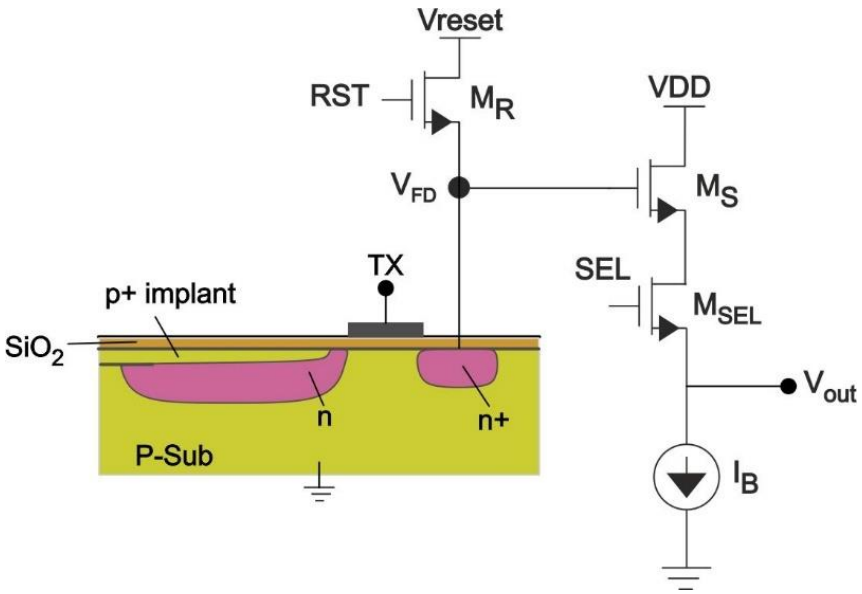

Fig. 4. 4T-APS pixel

The layout for this type of circuit, which is shown in Figure 5, is designed in a way that photodetectors are put on one side and the transistors are put on another part. It is desirable that most of the pixel area is occupied by the photodetector (A_{Pd}), and the rest of the space is allocated to transistors (A_C). The ratio of a pixel's light-sensitive area to its total area is a coefficient called fill-factor ($FF= A_{Pd}/(A_{Pd}+A_C)$). The higher the fill factor, the more sensitive a sensor is to light and would generate a clearer image in low light. A large number of transistors per pixel results in a low fill factor. Therefore, it is tried to include a fewer number of transistors in the pixel and to select transistors with the smallest possible size.

In the structure of the 4T-APS there are four transistors including pixel reset transistor (M_{RST}), charge transfer transistor (M_{TX}), amplifier transistor (M_S), and pixel selection transistor (M_{SEL}). To understand how 4T-APS works, we can consider its timing diagram which is shown in Figure 6.

At first, the voltage of the floating diffusion node FD is charged to V_{reset} by turning on $M_{RST,}$ and this voltage is sampled (outside the pixel array) as a reset voltage (V_{reset}). Afterwards, M_{TX} is turned on. As a result, the accumulation charge in the photodiode (Q_{sig}) decreases the voltage of the node FD as much as Q_{sig} /C_{FD} due to light. In this case, the pixel voltage is sampled as the signal voltage (V_{sig}) again. The result of subtracting these two sampled voltages ($V_{pix}=V_{reset}-V_{sig}$) is directly related to the incident light. This voltage is converted to digital code for storage.[2]

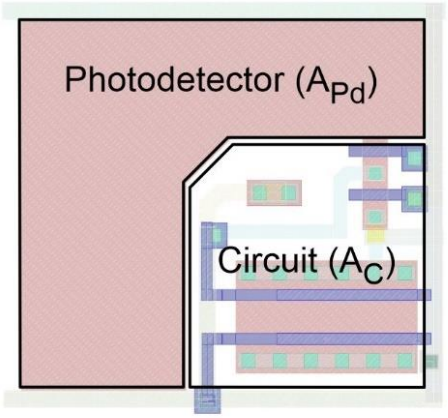

Fig. 5. Pixel silicon area divisions in the layout

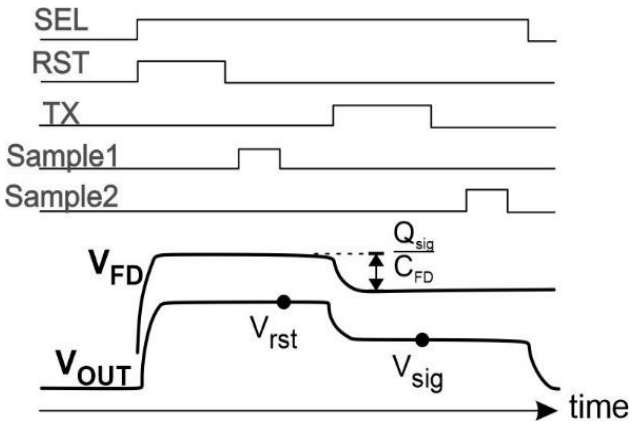

Fig. 6. the timing diagram of 4T-APS

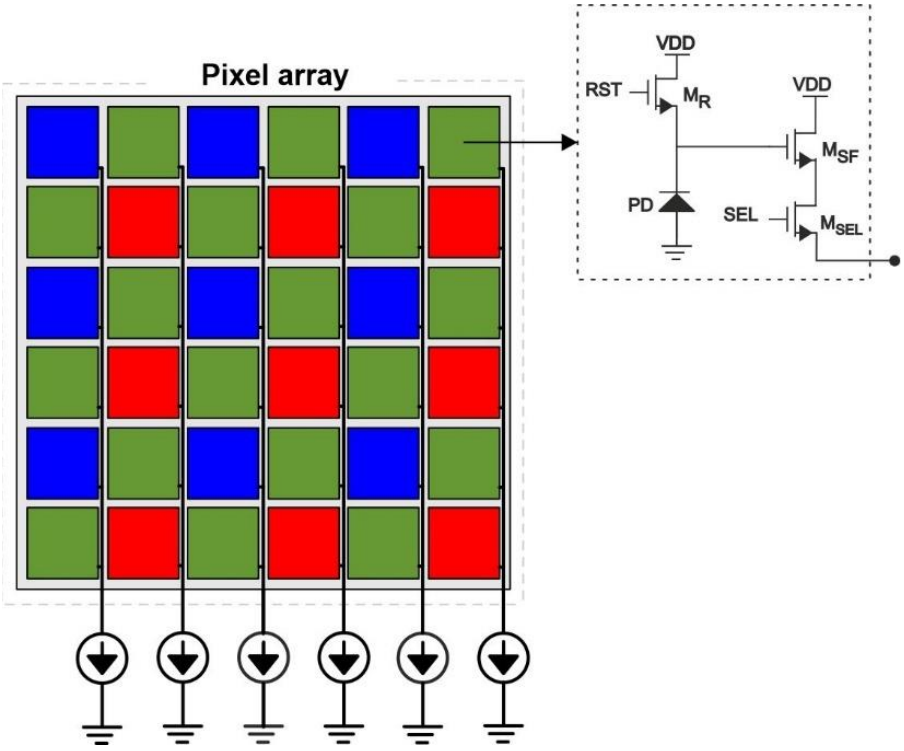

Fig. 7. 4T-APS connected to the column source follower

The most common and popular bias circuit for a 4T-APS is a current source. As shown in Figure 7, the current source is put outside the pixel array at the bottom of a column and each pixel voltage can be read by turning on the selection transistor (M_{SEL}) of the desired pixel. Note that when the transistor M_{SEL} is turned on, the amplifier transistor M_S with the current source $I_{B,}$ forms a CMOS source-follower (SF) circuit. Therefore, the voltage of the FD node is read by the SF circuit, which is called the pixel readout circuit. A simplified model of the pixel connected to the current source is presented in Figure 8.

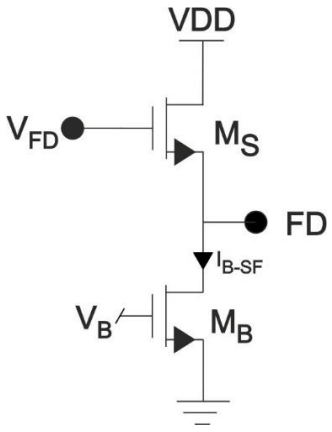

Fig. 8. CMOS source follower

As it can be seen, the input of the SF circuit is the voltage of the FD node and its output are available outside the array. According to the SF circuit, the equation below shows the relationship between the pixel output voltage and the voltage of the FD node:

where g_m and g_{mb} are the transconductance of the gate and bulk of M_S transistor. The reason why the SF circuit is so popular as a pixel readout circuit is the fact that it occupies low silicon area and power consumption, therefore it is abundantly used in image sensors. However, it has a non-linear manner and it causes the detector signal to be read as non-linear due to body effect and MOS channel length modulation, [10]. Many buffers have been offered to overcome the non-linear effects of the SF circuit, but the FF and power consumption has become a major challenge to them due to a large number of transistors [11-13].

3- A Proposed Method

According to the light theory, a color measurement requires at least three-color sensitivity to accurately represent an RGB code. As shown in Figure 2, the entire array is spread over a 2×2 block of pixels, and each color filter covers one-quarter of a block of pixels. As mentioned earlier, combining a 4T-APS with an SF circuit causes the photo-detector voltage to be read nonlinearly with attenuation. Using a voltage buffer inside the pixel can overcome these challenges, but the drawback is taking up too much space and thus reduces the FF drastically. Using the pixel sharing method and allocat-

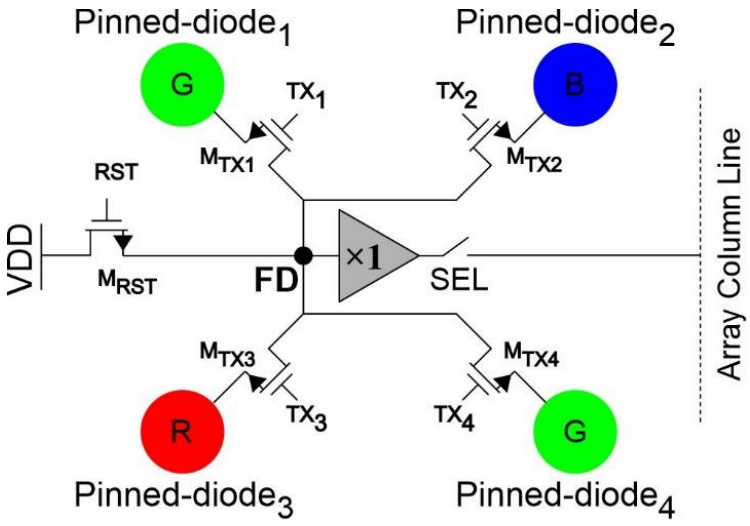

Fig. 9. the structure of the proposed pixel

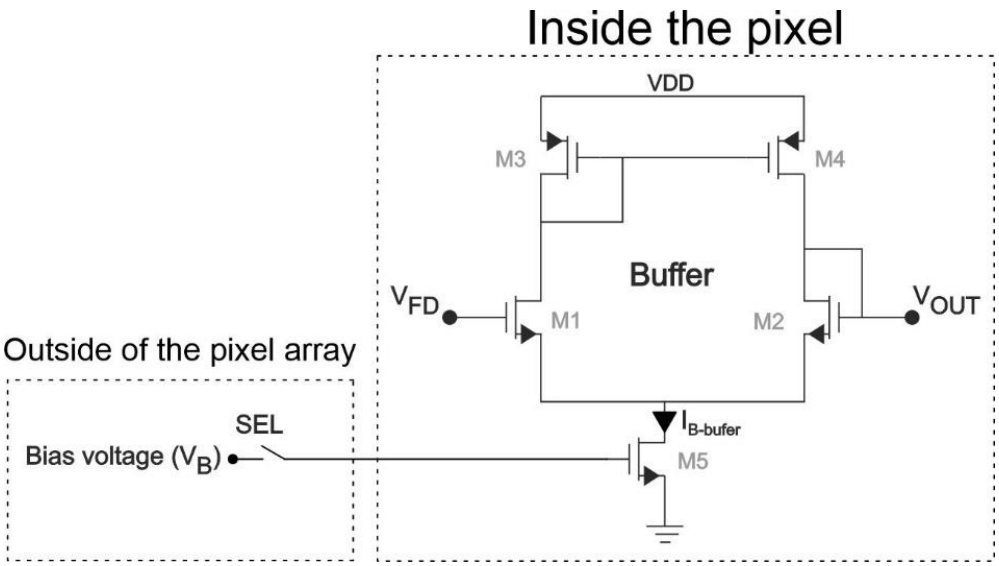

Fig. 10. the buffer circuit of the proposed pixel

ing one buffer for four adjacent pixels (Figure 9), the pixel voltages can be read with high linearity and high accuracy without losing the FF [14-17].

The voltage buffer circuit used in Figure 9 is a unity-gain buffer, using one stage differential amplifier that its circuit is shown in Figure 10. This circuit is connected to four adjacent Pinned-Photodiodes by transfer-gate transistors. To read the voltage of each Pinned-Photodiode, its transfer-gate transistor turns on and the other three transistors remain off. By applying an SEL pulse, the block of pixels is activated and each Pinned-Photodiode voltage can be directly read in reset or signal phases. The image sensor pixel array using the introduced pixel is shown in Figure 11.

4- Simulation Results

The proposed circuit is designed in 0.18µm CMOS technology and simulated by SPECTRE simulator. Various analyses, like frequency, transient, noise, and THD are performed to evaluate the proposed circuit and compare it with the conventional 4T-APS, which is connected to a constant current source. All the simulations were performed under the following conditions: SEL=V_{DD}, 0.2pF capacitive load, V_{DD}=1.8 V power supply, and $I_{B\text{-}SF}$= $I_{B\text{-}buffer}$≈10 µA bias currents. Table 1 indicates the dimensions of the transistors in the conventional and proposed circuits which are shown in Figures 8, 9, and 10. Based on the frequency simulation results, which are shown in Figure 12, voltage gains of the SF and the proposed

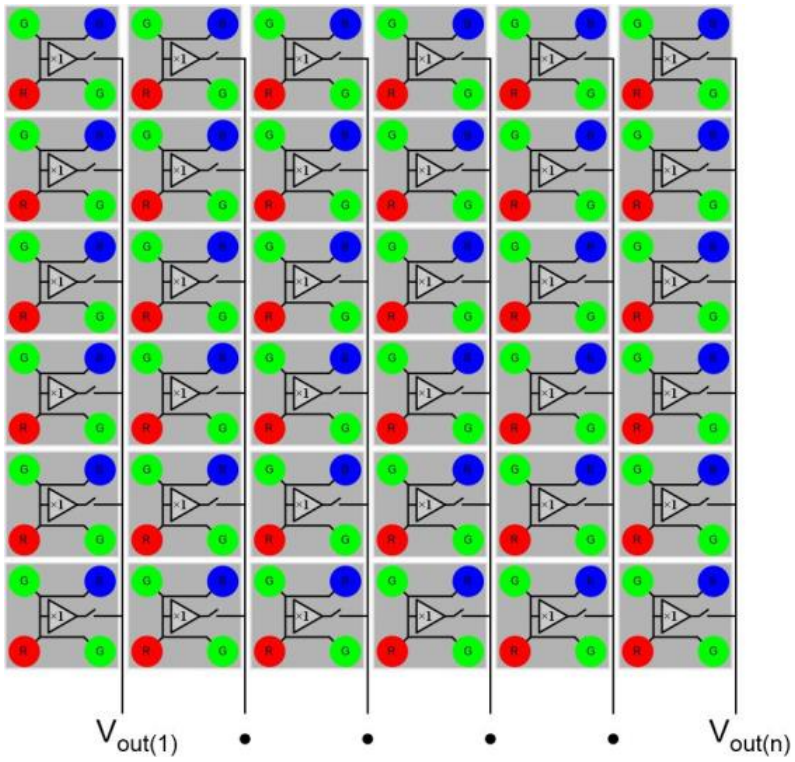

Fig. 11. Pixel array using the introduced pixel

Table 1 Dimensions of a transistors used in the circuits

Transistor	*W/L*
M_S	3µm/180nm
M_B, M_{rst}	220nm/180nm
M_{TX1} - M_{TX4}	220nm/180nm
M_1, M_2	3µm/180nm
M_3 - M_5	220nm/180nm

circuit are 0.8 and 0.96, respectively. As a result, a 16% improvement in voltage gain is obtained by the proposed circuit with the same power consumption as the SF.

To evaluate the linearity of the proposed and the conventional circuits, THD analysis was performed for both, and the results are shown in Figure 13.

As it can be seen, the buffer and SF have a linearity of 0.45% (-47 dB) and 1.42% (-37dB), respectively for the input amplitude of 0.4 V, meaning that the buffer is 10 dB more linear. By considering input swing ranges (V_{in}) from 0.6 to 1.4 V and the linearity of -47 dB in the output for the buffer and the SF circuits, the output voltage swings ($A_V \times V_{in}$) are obtained as 0.96 V and 0.64 V, respectively. It indicates a 33% decrease in the output swing for the SF. The results from the noise analysis of both circuits are shown in Figure 14, and the total input-referred noise of the buffer and the SF is obtained as 0.29mV and 0.22mV, respectively.

The step response of both circuits is shown in Figure 15. As it can be seen, the rising time for the buffer and the SF are 18 nS and 2 nS, respectively, indicatating the higher speed of the SF. Finally, the proposed pixel and source-follower readout circuit performance are shown in Table 2.

The layouts of the conventional pixel and the introduced pixel with a buffer are shown in Figure 16 and Figure 17, respectively.

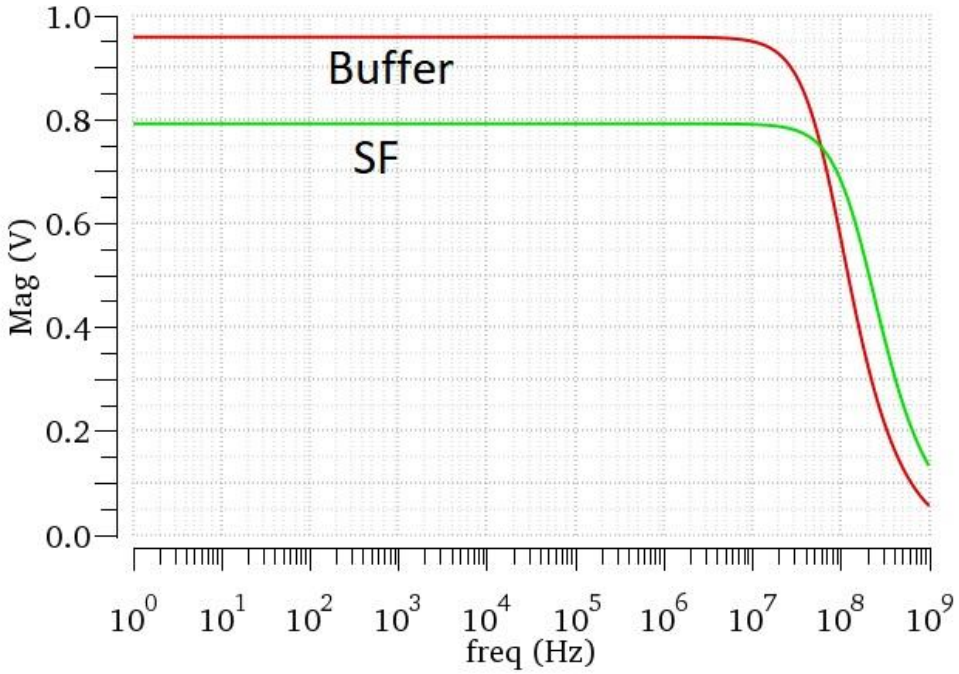

Fig. 12. Frequency response

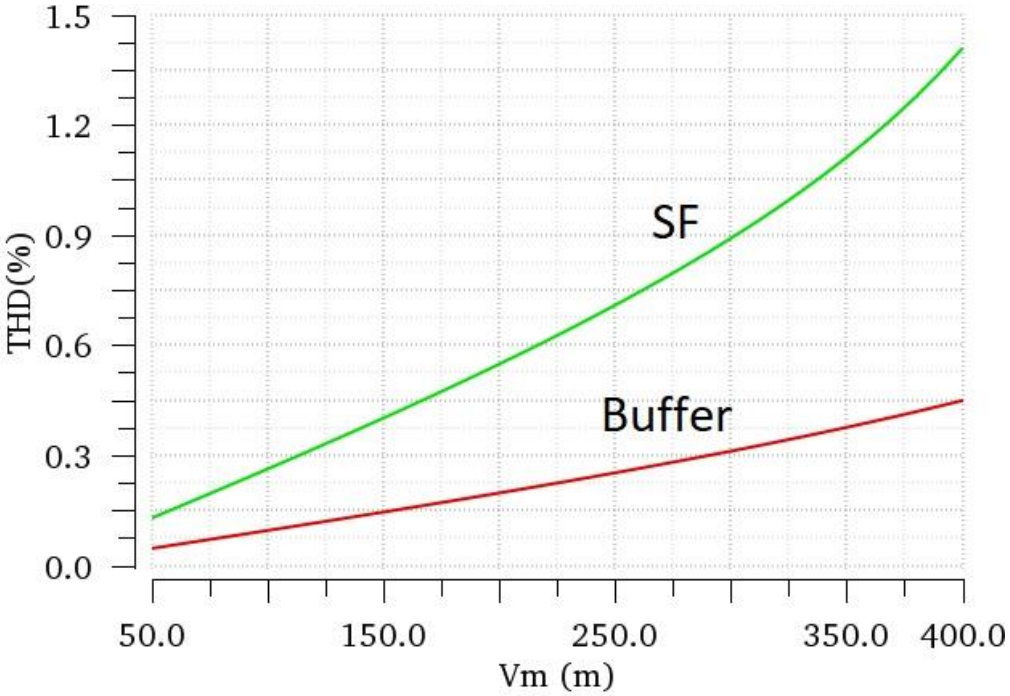

Fig. 13. THD analysis results

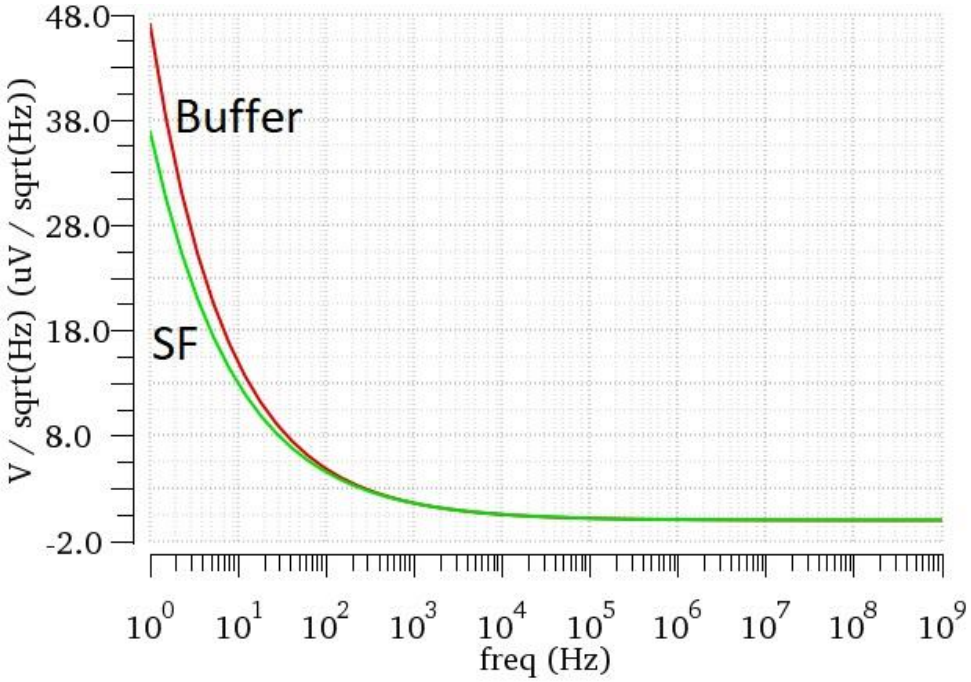

Fig. 14. Noise analysis

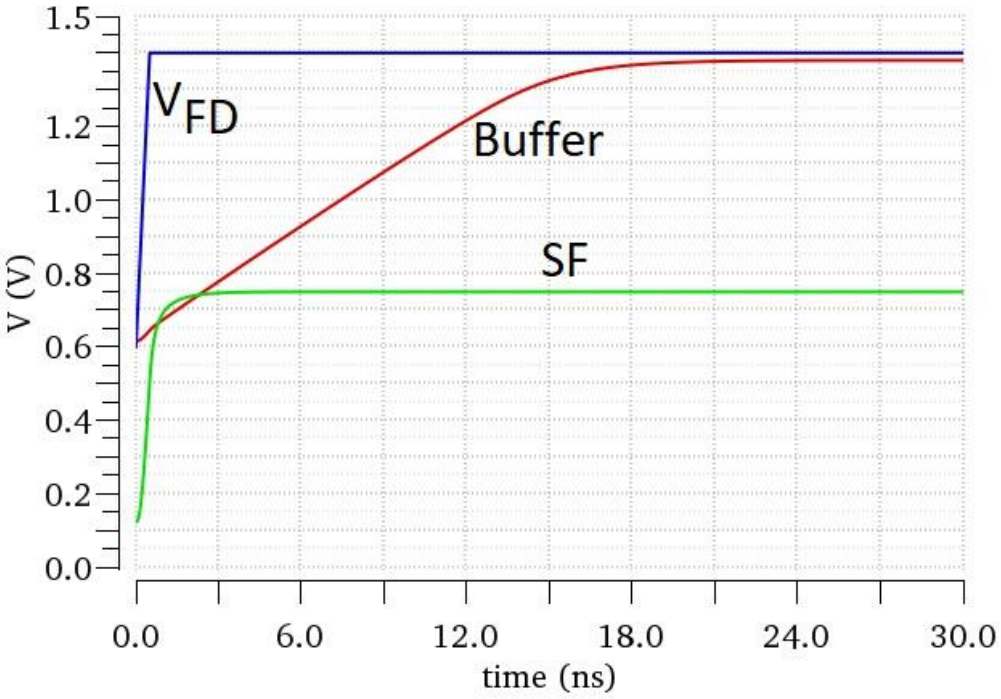

Fig. 15. Step response

Table 2. Performance comparison

	Proposed pixel	SF
Voltage gain	0.96	0.8
Linearirt @ 0.8V input range (%)	0.45	1.42
Total referred noise (mV)	0.29	0.22
Number of transistors @ four pixels	11	16
Fill Factor (%)	58	44
Rise time (nS)	18	2
Layout size (µm× µm)	14.8×14.8	7.4×7.4
Power supply (V)	1.8	1.8
Power consumption (µW)	16.8	18

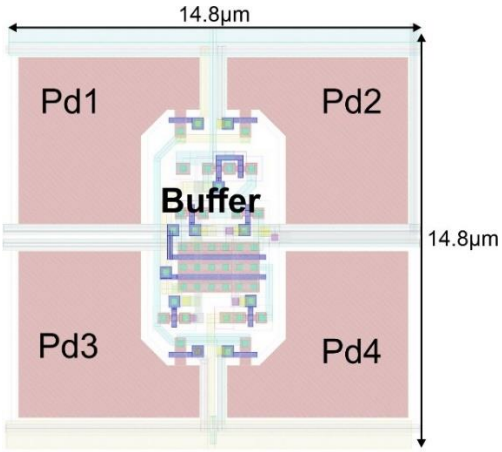

Fig. 16. The layout of pixels and a built-in buffer

5- Conclusion

An Active Pixel Sensor with a built-in voltage buffer is introduced in this paper, having considerable advantages compared to the conventional 4T-APS pixel which is connected to a constant current source. Both circuits are designed similarly regarding power consumption. Table 3 shows the performance summary and comparison of the proposed pixel with the previous works. With the proposed 4-shared pixel, it achieves a higher fill-factor in a status where the number of transistors per pixel and the line rate are intermediate.

Fig. 17. The layout of the 10×10 block pixel array

Table 3. Comparison with the previous sensors

Parameter	[18]	[19]	[20]	This work
Process (µm)	0.11	0.18	0.11	0.18
Pixel size(µm^2)	7.5×7.5	75×75	30×15	14.8 ×14.8
Fill factor (%)	52	-	47	58
Line rate (KHz)	9.62	0.45	100	40
Transistors per pixel	1.75	3	-	2.75
Readout circuit	SF	SF	Buffer	Buffer
Power supply (V)	3.3/1.5	-	3.3/1.5	1.8

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