

# Modified Space Vector Pulse Width Modulation for Three-Phase High Voltage Gain Switched-Inductor Split-Source Inverter

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**ABSTRACT:** Renewable energy sources, such as photovoltaic (PV) and fuel cells, have been given attention during the latest decades due to the limitations of non-renewable sources. Therefore, it is essential to improve the structure of voltage source inverters (VSIs) to increase their voltage gain in these applications. The split-source inverter (SSI) is a single-stage topology that uses the same number of power switches and switching states as VSI with boosting capability and the continuous input current. Three-phase switched-inductor SSI (SI-SSI) consists of two equal inductors, six diodes, one capacitor, and the bridge structure. This topology increases the voltage gain of conventional SSI. On the other hand, the modulation scheme impacts the inverters' performance. Space vector pulse width modulation (SVPWM) operates more efficiently than the third-harmonic injection pulse width modulation (THIPWM) and sinusoidal pulse width modulation (SPWM). However, varying the duty cycle of charging the inductors in each switching cycle increases the low-frequency ripples on the DC side of the inverter. To overcome the mentioned drawback in SVPWM, the modified SVPWM has been proposed. In the modified SVPWM, the interval corresponding to zero states is redistributed to charge both inductors of SI-SSI with similar constant duty cycles. Thus, the low-frequency components on the inductors' current and capacitor voltage are decreased without affecting the active states. The operation of three-phase SI-SSI with SPWM, THIPWM, traditional SVPWM, and modified SVPWM is investigated and simulated by MATLAB/Simulink.

## Review History:

Received: Feb. 15, 2023

Revised: Jun. 19, 2023

Accepted: Jul. 10, 2023

Available Online: Feb. 01, 2024

## Keywords:

Low-frequency ripples

Switched-inductor split-source in-  
verter (SI-SSI)

Sinusoidal PWM

Space vector PWM

Third-harmonic injection PWM

## 1- Introduction

Voltage source inverters (VSIs) are used frequently in renewable energy and industrial applications. Discontinuous input current and the buck operation mode are the main weaknesses of VSIs. However, the output voltage of photovoltaic arrays and fuel cells is low which should be boosted to the desired value and their output current should flow continuously. Three-phase SSI, shown in Fig. 1, overcomes these drawbacks without adding any power switches to the basic topology [1-4]. Also, it has a shorter commutation path, fewer passive elements count, and lower voltage stresses on semiconductors for higher voltage gains compared to Z-source inverters which is a well-known single-stage topology [1, 5].

Various topologies based on SSI are proposed to improve its operation by adding active and passive elements and reconfiguring its circuit [6-12]. However, in [6, 7, 9-11] the complexity of the proposed SSI structures is relatively high and the number of semiconductor switches is increased. Authors in [13] implemented the switched-inductor configuration on a single-phase SSI without adding any semiconductor switches. Two inductors with the same inductance and three diodes

compose the switched-inductor structure. In this paper, the inverter is controlled by sinusoidal pulse width modulation (SPWM), and a higher voltage gain than conventional SSI is reported. However, the operation of this topology is only investigated by this modulation method.

Space Vector PWM (SVPWM) provides better DC-link utilization, lower total harmonic distortion (THD) of output voltage, easier digital implementation, and higher efficiency than carrier-based modulations [14-17]. On the other hand, lower inductance and capacitance are required for SSI by SVPWM in comparison with other pulse width modulations [18]. However, due to the variable duty cycle of the inductor charging, the inductors' current and capacitor voltage have low-frequency components [12, 19].

A modified SVPWM has been proposed in [18] where the zero states are redistributed without affecting the active states to fix the duty cycle. This type of modulation enhances the converter performance by eliminating the low-frequency ripples on the inductors' current and the capacitor voltage through a different allocation of zero states in each switching cycle. It should be noted that the interval of the zero states is constant and it depends on the modulation index. A

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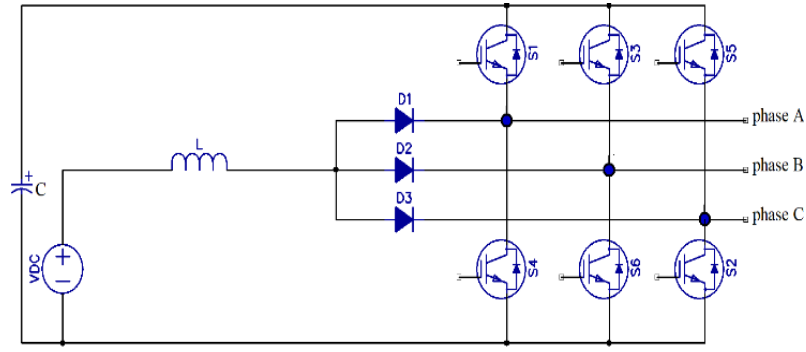


Fig. 1. Three-phase two-level SSI topology

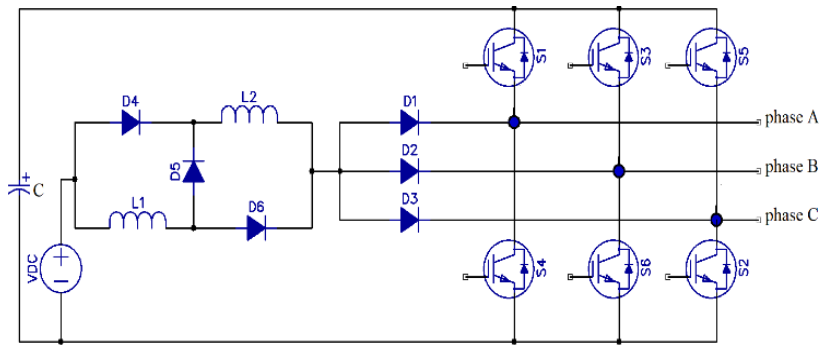


Fig. 2. Three-phase two-level switched-inductor split-source inverter SSI

similar concept is used for multidimensional pulse width modulation in [19]. Accordingly, the integration of SI-SSI with the modified SVPWM can provide some benefits that are considered in this paper.

This paper investigates and compares the operation of SI-SSI with SPWM, THIPWM, conventional SVPWM, and modified SVPWM approaches. It is organized as follows; the three-phase SI-SSI operation, modulation schemes, and mathematical derivations based on SPWM, THIPWM, and SVPWM are presented in sections 2 to 4, respectively. Then, SI-SSI is designed based on each modulation and simulated in section 5. Finally, section 6 concludes the paper.

## 2- SI-SSI by Sinusoidal PWM

### 2- 1- Operation

The structure of three-phase SI-SSI is shown in Fig. 2. Its configuration, during the charging and discharging states of inductors, is shown in Fig. 3 (a) and (b), respectively. Table 1 summarizes the switching states of this topology. In each leg, the lower and upper switches shouldn't be turned on simultaneously. During states (000) to (110), at least one of the lower switches ( $S_4$ ,  $S_6$ , and  $S_2$ ) is on, and thus, the input inductors are charged. In these states,  $D_4$  and  $D_6$  are biased

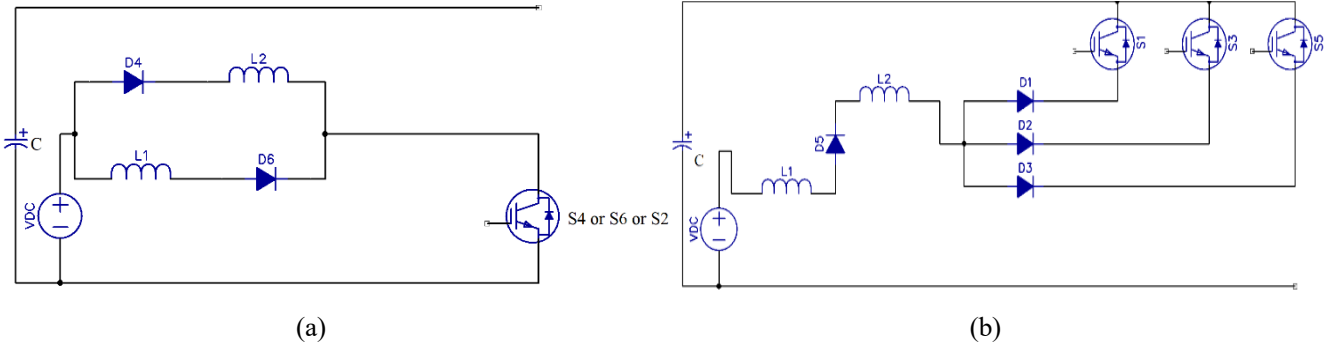
forward and  $D_5$  is reversed. Hence, inductors are parallel. In the state (111) in which all of the upper switches ( $S_1$ ,  $S_3$ , and  $S_5$ ) are on,  $D_5$  is on, and  $D_4$  and  $D_6$  are reverse biased. Thus, two series inductors are discharged into the DC-link capacitor.

By considering  $L_1$  and  $L_2$  are equal, the voltage of inductors can be calculated as (1) and (2) for charging and discharging states, respectively. The average voltage of inductors over a switching period is zero. As a result,  $V_C$  is derived as (3), where  $V_C$  is the average voltage across the capacitor, and  $V_{DC}$  is the input DC voltage. Also,  $D_{ave}$  is the average duty cycle of charging the inductors in a switching cycle.

$$V_{L1} = V_{L2} = V_{in} \quad (1)$$

$$V_{L1} = V_{L2} = \frac{V_{DC} - V_C}{2} \quad (2)$$

$$V_C = \frac{(1 + D_{ave})V_{in}}{(1 - D_{ave})} \quad (3)$$



**Fig. 3. The equivalent circuit of SI-SSI during, a) the charging states of input inductors, b) the discharging state of input inductors**

**Table 1. The switching states of SI-SSI**

States	S <sub>1</sub>	S <sub>3</sub>	S <sub>5</sub>	L <sub>1</sub> ,L <sub>2</sub>	C
(000)	off	off	off	charging	discharging
(001)	off	off	on	charging	discharging
(010)	off	on	off	charging	discharging
(011)	off	on	on	charging	discharging
(100)	on	off	off	charging	discharging
(101)	on	off	on	charging	discharging
(110)	on	on	off	charging	discharging
(111)	on	on	on	discharging	charging

**2- 2- Modulation scheme and mathematical derivations**

SSI can be controlled by any modulation scheme of VSIs. In SPWM, when the reference signal is greater than the carrier wave, the upper switch of the corresponding phase is turned on. The state (111) occurs when the carrier wave is smaller than all the reference signals. The interval of this state changes during the fundamental cycle and thus, L<sub>1</sub> and L<sub>2</sub> will be charged with the variable duty cycle of D. This duty cycle varies with a low frequency of three times the fundamental frequency (f<sub>1</sub>) [1]. The duty cycle is given by (4) in terms of θ where θ=2πf<sub>1</sub>t, 7π/6 ≤ θ ≤ 11π/6 and M is the modulation index. The inductor is charged with an average duty cycle of D<sub>ave</sub> which can be determined as (5) by averaging (4) over the range of 7π/6 ≤ θ ≤ 11π/6.

$$D(\theta) = \frac{1}{2} - \frac{M}{2} \sin(\theta) \tag{4}$$

$$D_{ave} = \frac{3\sqrt{3}M}{4\pi} \tag{5}$$

By substituting (5) in (3), the DC-link voltage of the inverter, V<sub>C</sub> can be obtained as (6). Also, the fundamental peak of the phase voltage, V<sub>φ1</sub>, is presented as (7) which is obtained by multiplying (6) and (M cos(φ)) / 2.

$$V_C = \frac{(6\pi + 3\sqrt{3}M)V_{DC}}{(2\pi - 3\sqrt{3}M)} \tag{6}$$

$$V_{\phi 1} = \frac{(3\sqrt{3}M^2 + 6\pi M)V_{DC} \cos(\varphi)}{(4\pi - 6\sqrt{3}M)} \tag{7}$$

The ripple values of the inductors' current (Δi<sub>L</sub>) and the capacitor voltage (ΔV<sub>C</sub>) are given by (8) and (9) which include high-frequency and low-frequency terms [1]. The low-frequency ripples of inductors' current (Δi<sub>Ll</sub>) and capacitor voltage (ΔV<sub>Cl</sub>) are caused by the duty cycle variation [1, 18]. Δi<sub>Lh</sub> and ΔV<sub>Ch</sub> are high-frequency ripples on the inductor current and the capacitor voltage which are caused by switching the semiconductors. In the discharging

state, the low-frequency component of the inductors voltage  $|V_{Ll}|$  and the capacitor current  $|I_{Cl}|$  are given by (10) and (11), respectively where  $I_L$  is the average current of inductors.

$$\Delta I_L = \Delta I_{Ll} + \Delta I_{Lh} = \frac{|v_{Ll}|}{3\omega_l L} + \frac{DV_{DC}}{f_s L} \quad (8)$$

$$\Delta V_L = \Delta V_{Ll} + \Delta V_{Lh} = \frac{|I_{Cl}|}{3\omega_l C} + \frac{(1-D)I_L}{f_s C} \quad (9)$$

$$|v_{Ll}| = \frac{(1-D(\theta))V_C}{2} \quad (10)$$

$$|I_{Cl}| = (1-D(\theta))I_L \quad (11)$$

For obtaining the low frequency of  $D(\theta)$ , the fundamental term of the Fourier series of  $D(\theta)$  is calculated and given by (12) [18]. By substituting (12) in (8) to (11), the required inductance ( $L$ ) and capacitance ( $C$ ) are derived as (13) and (14), respectively.  $D_{max}$  and  $D_{min}$  are the maximum and minimum duty cycles in the mentioned range of  $\theta$ , respectively.

$$D_l = \frac{3\sqrt{3}M}{8\pi} \quad (12)$$

$$L \approx \frac{\sqrt{3}MV_C}{32\pi^2 f_1 \Delta i_L} + \frac{D_{max} V_{DC}}{f_s \Delta i_L} \quad (13)$$

$$C \approx \frac{\sqrt{3}MI_L}{16\pi^2 f_1 \Delta V_c} + \frac{(1-D_{min})I_L}{f_s \Delta V_c} \quad (14)$$

### 3- SI-SSI by Third-Harmonic Injection PWM

THIPWM is one of the standard PWM schemes in which a third harmonic of the sinusoidal signal with a coefficient of 1/6 is added to the reference wave. It utilizes the DC-link voltage more efficiently and decreases low-frequency harmonics in comparison with SPWM [1, 18]. The duty cycle is presented in (15) in terms of  $\theta$  and  $M$  where  $7\pi/6 \leq \theta \leq 11\pi/6$  [1]. Using the aforementioned range of  $\theta$  and (15), the average duty cycle can be derived as (16).

$$D(\theta) = \frac{1}{2} - \frac{M}{\sqrt{3}} (\sin(\theta) + \frac{1}{6} \sin(3\theta)) \quad (15)$$

$$D_{ave} = \frac{1}{2} + \frac{3M}{2\pi} \quad (16)$$

By replacing (16) in (3), the DC-link voltage of the inverter,  $V_C$ , is attained as (17). Also,  $V_{\phi 1}$  is presented in (18) which is obtained by multiplying (17) and  $(M \cos(\varphi))/\sqrt{3}$ .

$$V_C = \frac{(3\pi + 3M)V_{DC}}{(\pi - 3M)} \quad (17)$$

$$V_{\phi 1} = \frac{(3\pi M + 3M^2)V_{DC} \cos(\varphi)}{(\sqrt{3}\pi - 3\sqrt{3}M)} \quad (18)$$

Similar to the SPWM scheme, the ripple values of the inductors' current ( $\Delta i_L$ ) and the capacitor voltage ( $\Delta V_C$ ) are given by (19) and (20).

$$\Delta I_L = \Delta I_{Ll} + \Delta I_{Lh} = \frac{|v_{Ll}|}{3\omega_l L} + \frac{DV_{DC}}{f_s L} \quad (19)$$

$$V_L = \Delta V_{Ll} + \Delta V_{Lh} = \frac{|I_{Cl}|}{3\omega_l C} + \frac{(1-D)I_L}{f_s C} \quad (20)$$

For obtaining the low frequency of  $D(\theta)$ , the fundamental term of the Fourier series of  $D(\theta)$  is given by (21). By substituting (21) in (19) and (20), similar to the calculated process in SPWM, the required inductance ( $L$ ) and capacitance ( $C$ ) are derived as (22) and (23), respectively.

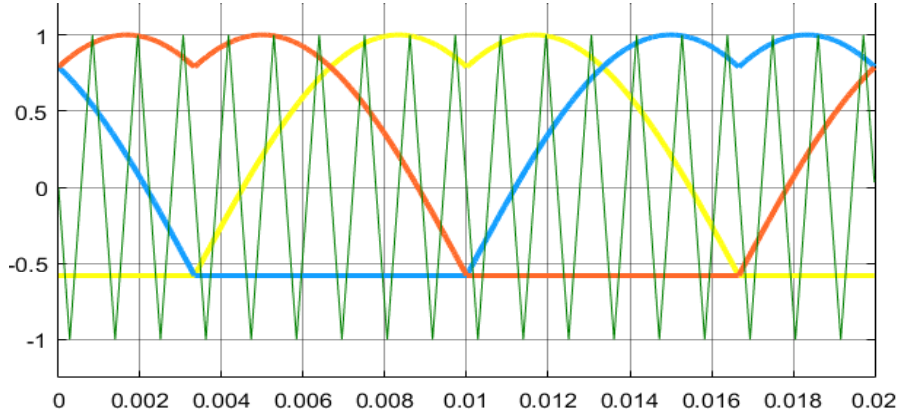
$$D_l = \frac{27 - 4\pi\sqrt{3}M}{36\pi} \quad (21)$$

$$L \approx \frac{V_C}{16\pi^2 f_1 \Delta i_L} - \frac{\sqrt{3}MV_C}{108\pi f_1 \Delta i_L} + \frac{D_{max} V_{DC}}{f_s \Delta i_L} \quad (22)$$

$$C \approx \frac{I_L}{8\pi^2 f_1 \Delta V_c} - \frac{\sqrt{3}MI_L}{54\pi f_1 \Delta V_c} + \frac{(1-D_{min})I_L}{f_s \Delta V_c} \quad (23)$$

### 4- SI-SSI by Space Vector PWM

SVPWM provides a quasi-sinusoidal output voltage with less THD and better DC-link utilization. In SVPWM, the three-phase reference voltages are transformed into two components in the stationary frame. Thus, by considering eight switching states, eight different vectors are produced [14-17]. Similar to SPWM, when the reference signal is greater than the carrier wave, the upper switch of the corresponding phase is on otherwise the switch is off.



**Fig. 4. Reference and carrier signals for the modified SVPWM scheme**

#### 4- 1- Conventional SVPWM

Similar to SPWM, the duty cycle of conventional SVPWM is not constant, and it varies with a low frequency equal to six times the fundamental frequency. For this modulation scheme,  $D$  and  $D_{ave}$  are given by (24) and (25), respectively where  $0 \leq \theta \leq \pi/3$  [20, 21]. Therefore, the DC-link voltage is calculated as (26). Also, the phase voltage  $V_{\phi 1}$  can be obtained by multiplying (17) by  $(M \cos(\varphi))'$  which is given by (27).

$$D(\theta) = \frac{1}{2} - \frac{M}{2} \sin(\theta - \frac{2\pi}{3}) \quad (24)$$

$$D_{ave} = \frac{1}{2} + \frac{3M}{2\pi} \quad (25)$$

$$V_C = \frac{(3\pi + 3M)V_{DC}}{(\pi - 3M)} \quad (26)$$

$$V_{\phi 1} = \frac{(3M^2 + 3\pi M)V_{DC} \cos(\varphi)}{(\sqrt{3}\pi - 3\sqrt{3}M)} \quad (27)$$

In SVPWM,  $\Delta I_L$  and  $\Delta V_C$  are given by (28) and (29). For obtaining the low-frequency component of  $D(\theta)$ , the fundamental term of the Fourier series of  $D(\theta)$  is calculated and given by (30) [18]. Thus, the required L and C for restricting ripples are calculated in (31) and (32). As seen, by SVPWM, the low-frequency ripples are much smaller than those in SPWM.

$$\Delta I_L = \Delta I_{Ll} + \Delta I_{Lh} = \frac{|V_{Ll}|}{6\omega_l L} + \frac{DV_{DC}}{f_s L} \quad (28)$$

$$\Delta V_L = \Delta V_{Ll} + \Delta V_{Lh} = \frac{|I_{Cl}|}{6\omega_l C} + \frac{(1-D)I_L}{f_s C} \quad (29)$$

$$D_l = \frac{6M}{35\pi} \quad (30)$$

$$L \approx \frac{MV_{inv}}{140\pi^2 f_1 \Delta I_L} + \frac{D_{max} V_{DC}}{f_s \Delta I_L} \quad (31)$$

$$C \approx \frac{MI_L}{70\pi^2 f_1 \Delta V_C} + \frac{(1-D_{min})I_L}{f_s \Delta V_C} \quad (32)$$

#### 4- 2- Modified SVPWM

In the conventional SVPWM, the variable duty cycle causes large low-frequency ripples on the current of the inductors and the voltage of the capacitor. In [18], for SSI, the interval of state (111) is kept constant and determined as (33). Thus, the interval of the state (000) is given by (34) where  $T_z$  is the total interval of zero states and  $T_{z0}$  represents the equivalent time of the state (000). The Reference and carrier signals in the modified SVPWM scheme are shown in Fig. 4.

$$T_{z1} = t_{off} = T_s(1-M) \quad (33)$$

$$T_{z0} = T_z - T_{z1} \quad (34)$$

Therefore, the duty cycle of inductors' discharging is constant and equal to the modulation index. The voltage of the capacitor is given by (35), and finally, the fundamental

**Table 2. The results of designing a 6 kW SI-SSI**

$V_{DC}$	$I_{L1}, I_{L2}$	$V_{\phi 1}$	$I_{\phi 1}$	$P.F.$	$R_{load}$	$L_{load}$	$f_s$	$f_1$
100 V	43 A	$220\sqrt{2}$ V	$11.38\sqrt{2}$ A	0.8Lag	19.37 $\Omega$	46.24 mH	15 kHz	50 Hz

	$M$	$V_C$	$L_1, L_2$	$C$
SPWM	0.7723	1007.07 V	21.21 mH	495.38 $\mu$ F
THIPWM	0.6688	1007 V	13.68 mH	283.77 $\mu$ F
modified SVPWM	0.6688	1006.98 V	3.56 mH	180 $\mu$ F
SVPWM	0.79	852.38 V	3.49 mH	150 $\mu$ F

amplitude of the phase voltage ( $V_{\phi 1}$ ) can be obtained according to (36).

$$V_C = \frac{(1+M)V_{DC}}{(1-M)} \quad (35)$$

$$V_{\phi 1} = \frac{(M^2 + M)V_{DC} \cos(\varphi)}{(\sqrt{3} - \sqrt{3}M)} \quad (36)$$

By substituting  $M$  in (28) and (29), the inductance of inductors and the capacitance of DC-link can be derived as (37) and (38) for SI-SSI. As seen, the low-frequency ripples cannot be quite removed [12]. Thus, the low-frequency component in (37) and (38) should not be neglected. However, the integration of the switched-inductor SSI structure and modified SVPWM provide higher voltage gain with smaller inductance and capacitance for the impedance network.

$$L_1 = L_2 = \frac{MV_{inv}}{140\pi^2 f_1 \Delta I_L} + \frac{MV_{DC}}{f_s \Delta I_L} \quad (37)$$

$$C = \frac{MI_L}{35\pi^2 f_1 \Delta v_C} + \frac{(1-M)I_L}{f_s \Delta v_C} \quad (38)$$

### 5- The Inverter Design and Simulation Results

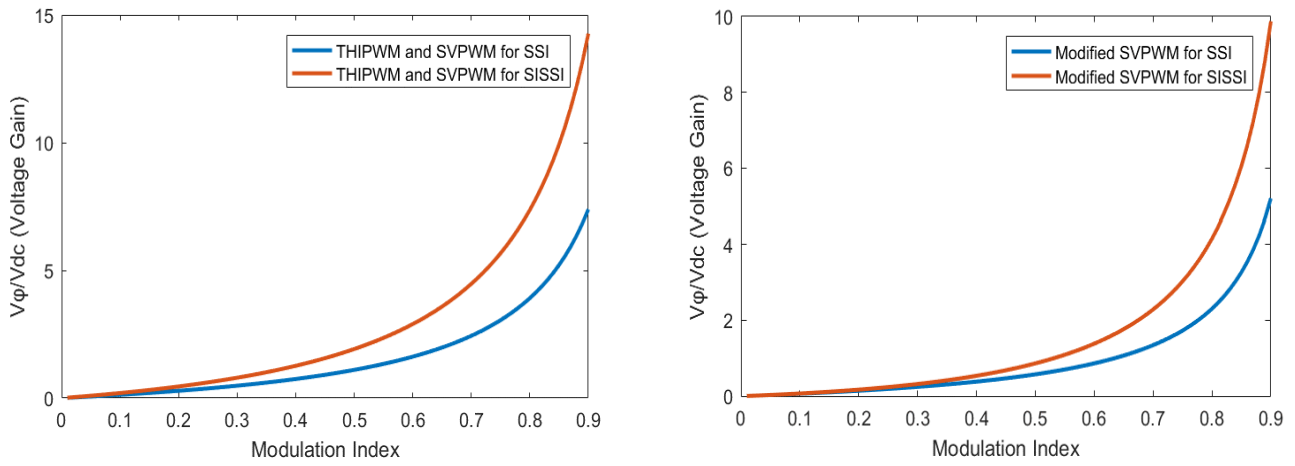
In this section, the power circuit design and simulation results of a 6 kW SI-SSI are presented. It is assumed that the

inverter is fed by a 100V DC input voltage. The fundamental amplitude of the phase voltage is equal to 220 V and its frequency is 50Hz. By considering a 10% ripple on the current of inductors and a 2% ripple on the DC-link voltage, the required inductance and capacitance will be calculated. The results of the converter design for each modulation scheme are listed in Table 2. According to Table 2, the modified SVPWM has the least values of inductance, capacitance, and DC-link voltage between these control approaches.

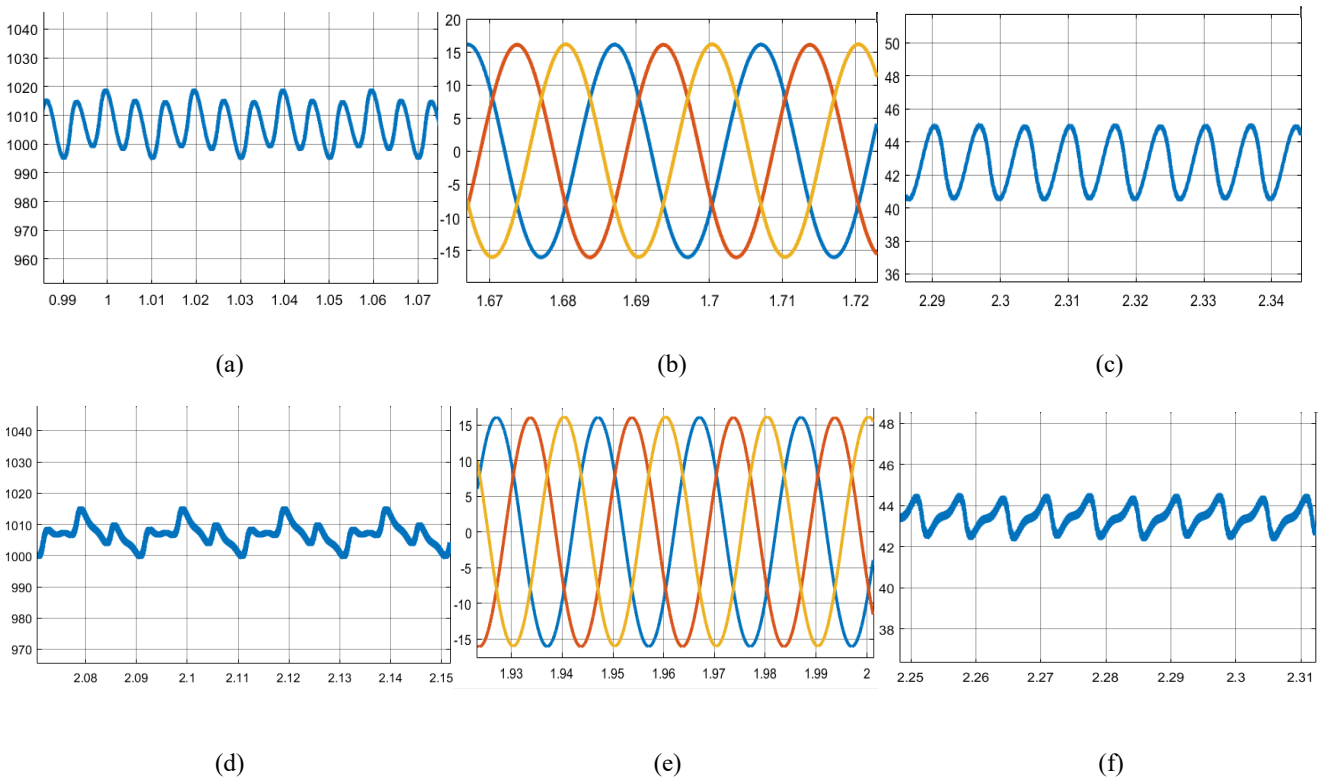
A comparison study for  $V_{\phi 1}/V_{DC}$  versus  $M$  for SSI and SI-SSI topologies is shown in Fig. 5. These inverters are controlled by THIPWM as well as traditional and modified SVPWM schemes and the power factor is unity. As seen, under the similar modulation index and input DC voltage, SI-SSI gives higher voltage gain for THIPWM, SVPWM, and modified SVPWM modulations. In other words, SI-SSI requires less input DC voltage than SSI for generating a specified output voltage. As seen, by modified SVPWM, the low-frequency components are reduced and the lowest passive elements are obtained. In addition, a smaller DC-link voltage is achieved when the modified SVPWM scheme is used for SI-SSI.

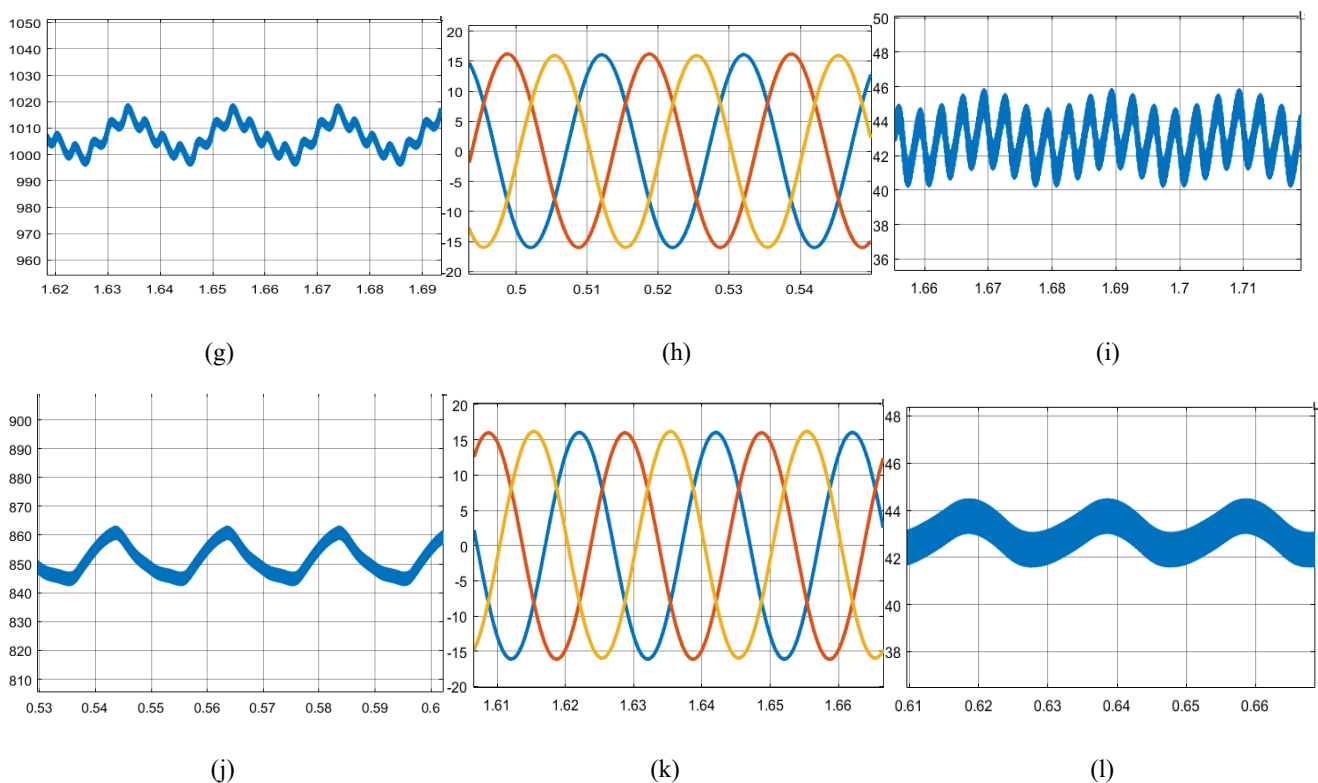
The simulation results of this topology with MATLAB/Simulink based on SPWM, SVPWM, and modified SVPWM are shown in Fig. 6. According to Fig. 6, simulation results verify the theoretical analysis. By the modified SVPWM, the peak-to-peak values of low-frequency ripple on the DC-link voltage and inductors' current are 5 V and 2.5 A less than SPWM and SVPWM schemes, respectively. Although the peak-to-peak low-frequency ripples for the modified SVPWM and THIPWM schemes are the same, the modified SVPWM provides the least DC-link voltage, voltage stress on semiconductors, inductance, and capacitance.





**Fig. 5.  $V_{\phi_1}/V_{DC}$  versus  $M$  for SSI and SI-SSI topologies controlled by SVPWM and modified SVPWM**





**Fig. 6.** SI-SSI simulation results of (a), (d), (g), and (j) inverter DC-link voltage, (b), (e), (h), and (k) load current, and (c), (f), (i), and (l) inductors current by SPWM, THIPWM, SVPWM, and modified SVPWM schemes, respectively.

## 6- Conclusion

This paper investigated the operation of a three-phase high gain switched-inductor split-source inverter (SI-SSI) with SPWM, THIPWM, SVPWM, and modified SVPWM control methods. The mathematical equations of SI-SSI such as voltage gain and components design are analyzed and derived for each modulation scheme. As seen, SI-SSI based on the modified SVPWM requires smaller inductance, capacitance, and DC-link voltage in comparison with SPWM, THIPWM, and SVPWM while higher voltage gain can be achieved. In other words, by the modified SVPWM, low-frequency components are decreased by fixing the duty cycle, and the peak-to-peak low-frequency ripples of DC-link voltage and inductors' current for the modified SVPWM are smaller than SPWM and the conventional SVPWM schemes. Thus, it can be assumed as a merit for renewable resources such as PV and fuel cell applications, as their output voltages are low. Also, SI-SSI was simulated in MATLAB/Simulink for the four mentioned modulations. The results validate the operation of this topology with the proposed PWMs.

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#### HOW TO CITE THIS ARTICLE

M. Salehizadeh, S. H. Montazeri, J. Milimonfared, H. Rastegar, *Modified Space Vector Pulse Width Modulation for Three-Phase High Voltage Gain Switched-Inductor Split-Source Inverter*, AUT J Electr Eng, 56(1) (Special Issue) (2024) 141-150.

DOI: [10.22060/ej.2023.22190.5522](https://doi.org/10.22060/ej.2023.22190.5522)



