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A CMOS 3.5 GHz Bandwidth Low Noise Amplifier using Active Inductor

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Abstract:

This paper presents a 3.5 GHz bandwidth wideband low noise amplifier (LNA) with low power consumption, high power gain, and acceptable linearity in 130 nm CMOS technology for use as a separate chip. The LNA includes two parallel branches: a gm-boosted common-gate (CG) path and a common-source (CS) current reuse path. The CG path handles wideband input impedance matching, while the CS path is utilized to achieve enough power gain and enhance linearity. The noise cancellation technique is adopted to reduce the noise generated by the gm-boosted CG stage and linearity is taken care of by choosing suitable gain values for CG and CS. Also, an active inductive shunt-peaking technique is used to increase the bandwidth to 3.5 GHz. The post-layout simulation results of the circuit in 130 nm CMOS technology show that in the whole bandwidth of 0.25 GHz to 3.75 GHz the power gain, noise figure, and third-order input intercept point (*IIP3*) are 15±1 dB, 2.25±0.3 dB, and -5.5 dBm, respectively. Also, the S11 and S22 are less than -15 dB and -19 dB, which is adequate for an LNA integrated circuit. The proposed LNA consumes 4.7 mW with a 1 V power supply and occupies an area of 0.047 mm2.

Keywords:

Low noise amplifier (LNA), Broadband Amplifier, CMOS, Noise Cancellation, Linearity

1. Introduction

With the increasing number of wireless standards, the need for multi-standard transceivers or so-called "Universal Receivers" is growing. Today, a wireless communication chip must cover several standards such as WCDMA, WLAN, DVB-T/T2, GPS, FM radio, and Cognitive radio. For example, a mobile phone

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must be able to receive digital TV, radio, GSM, and Wi-Fi signals simultaneously. Therefore, the front-end circuits of the universal receiver have to be able to accommodate operations across a wide range of frequency bands and different performance requirements for low noise amplifiers (LNA). The main parameters of an LNA include bandwidth, input return loss, noise figure, linearity, and power gain [1]. There is a trade-off between these parameters and the power consumption. On the other hand, new portable systems or battery-less devices require very low power-consumption circuits [2]. Thus, the main challenges facing these systems are noise figure (NF) and linearity, and the achievement of an ultra-low power design to operate for several days (for mobile phones) or even a year (for medical devices) by using a single Lithium-Ion battery [3]. Some circuit methods, e.g., noise cancellation and current-reuse techniques, simultaneously reduce NF and power consumption [4, 5]. The authors in [6] used an inductor between the gate of the cascode transistor and the power supply to improve the *IIP3* of a sub-threshold LNA. Although using the passive inductor improved the *IIP3*, the occupied area of the chip is slightly large. In [7] a noise-canceling balun CG- CS LNA is employed in the frequency range of 0.4-3.4 GHz. In [8], using a CS circuit with the noise cancellation technique in parallel with a CG path, a bandwidth of 1.7 GHz and *IIP3* of about 0.25 dBm are achieved in 180 nm technology. Although the circuit is inductor-less and therefore small in area, the NF is high.

Inductive series or parallel peaking method is commonly used in broadband LNA. Due to the use of an inductor, this method suffers from the requirement of a large occupied area on the chip [9]. Using active inductors (AI) reduces the total chip area, but the noise, linearity, and power consumption should be carefully considered [10-12]. The authors in [13] used an AI in a narrow-band circuit and achieved a good power gain and noise figure, but the *IIP3* and frequency bandwidth are low.

This paper presents a wide-band LNA with a bandwidth of 0.25 GHz to 3.75 GHz with a power gain of 15±1 dB, a noise figure less than 2.5 dB, and *IIP3* of -5.5 dBm. The return losses in input and output are less than -15 dB and -19 dB, while the power consumption from a 1V power supply is 4.7 mW. The proposed LNA consists of two parallel stages: a gm-boosted CG input stage and a CS stage using a current-

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reuse technique. The gains in the two parallel stages have been selected to simultaneously achieve noise cancellation and good linearity. The CG input stage provides a wideband input matching. In addition, an active inductive shunt-peaking technique has been used to enhance the bandwidth to 3.5 GHz.

This paper is organized as follows: Section 2 introduces and analyzes the proposed broadband LNA circuit, including AI analysis, input impedance, gain, noise, and linearity. Section 3 gives the post-layout simulation results and comparisons with similar recent works. The conclusion is given in Section 4.

2. Analysis of proposed LNA

Fig. 1 shows the proposed circuit and its components. According to the figure, the circuit is composed of four different parts, which include bias circuits, common gate amplifier with gm-boosting, main amplifier

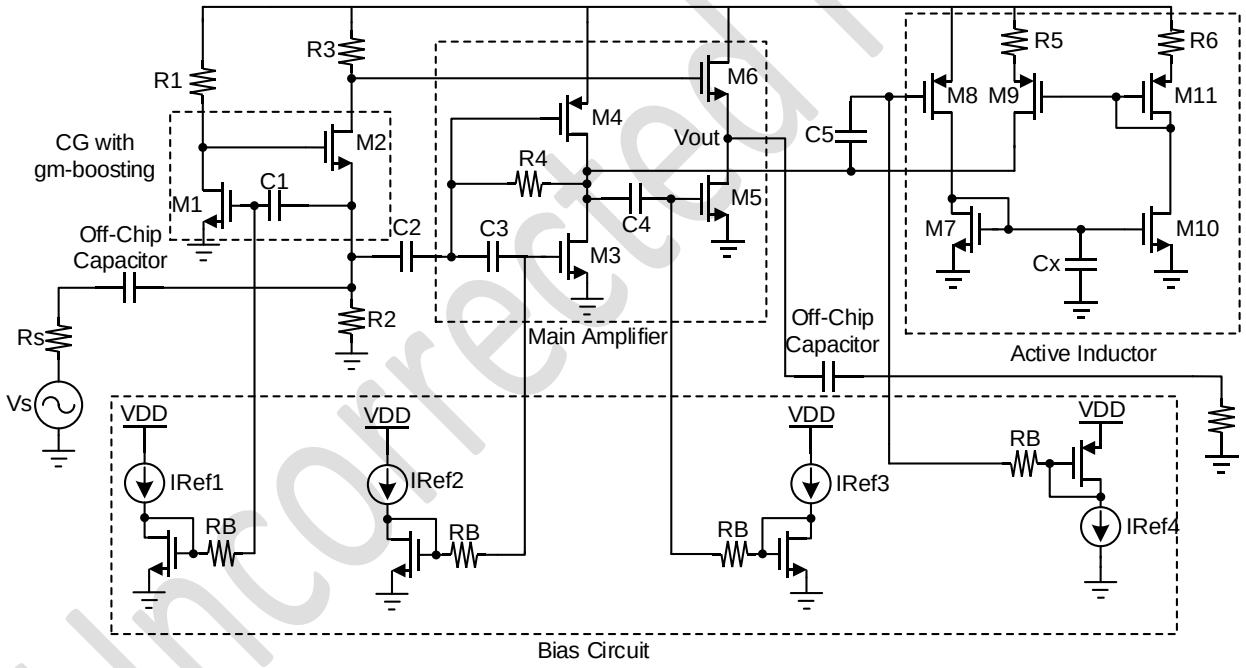

Fig. 1. The schematic of the proposed LNA

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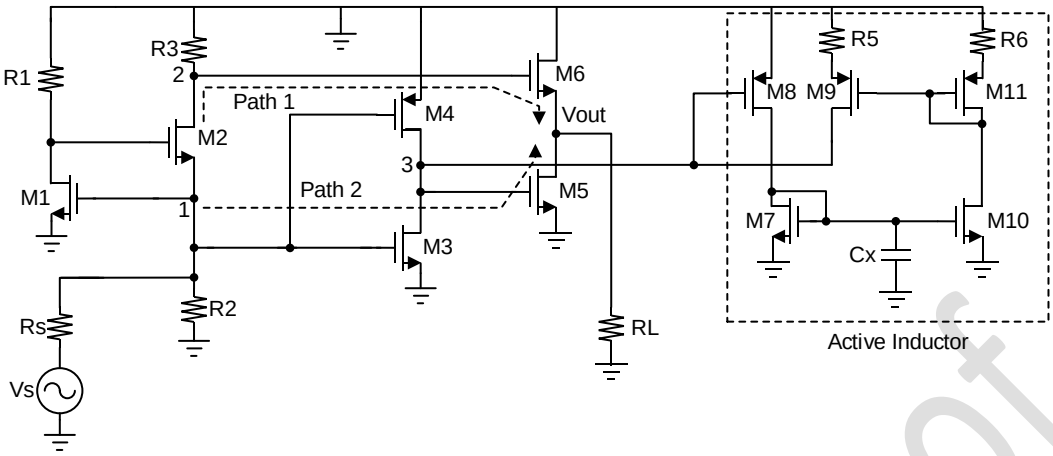

Fig. 2. The AC equivalent of the proposed LNA

consisting of two stages of common source with current-reuse technique, and AI circuits. AC equivalent of the proposed circuit is shown in Fig. 2.

A large resistor R4 is used to determine the DC voltage of drain M4 and M3 and is therefore ignored in the AC analysis. Also, the DC current of M2 is very small therefore, we choose a very large R2 to ignore it in the AC equivalent circuit. The gm-boosting CG stage composed of M1 and M2 aims to provide a wide input impedance matching. The DC current and in turn, the transconductance of M2 is low (due to reducing the

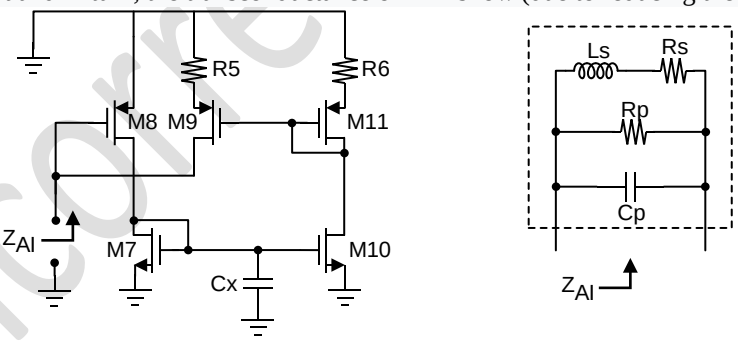

Fig. 3. AI with its equivalent circuit

power consumption) thus, the gm-boosting technique is utilized to enhance the gain by using transistor M1 and resistor R1. By investigating the noise voltages of the gm-boosting circuit and transistor M2 at node 1 and node 2, and the signal at the mentioned nodes in Fig. 2, the signal voltage polarity of node 1 and node 2 is the same, while the noise voltage polarity is inverted. The procedure to remove the mentioned noise is

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explained in detail in the “Noise Analysis” section. Also, an AI network with very low power consumption has been used to enhance the bandwidth by using the shunt-inductive peaking technique.

2-1- The Active Inductor Analysis

Fig. 3 shows the proposed active inductor circuit and its equivalent circuit. The DC currents in M8, M10, and M11 are very low; hence the ro_8, ro_{10}, and ro_{11} of the small signal model can be ignored. The input impedance is expressed as follows:

$$\frac{1}{ZAI}=\left(\frac{1}{\left(1+gm_9R_5\right)ro_9}+\frac{gm_8gm_9gm_{10}ro_9ro_{11}\left(1+gm_{11}R_6\right)}{\left(1+gm_{11}ro_{11}\right)\left(1+gm_9R_5\right)ro_9\left(j\omega C_T+gm_7\right)}+j\omega\left(Cgs_8+\left(1+\frac{gm_8}{gm_7}\right)Cgd_8\right)\right) \tag{1}$$

where C_T is defined as $C_T=Cx+Cgs_7+Cgs_{10}$. Given that Cx is much larger than others, then $C_T\approx Cx$.

Based on Eq. (1), the equivalent of AI is depicted in Fig. 3 where L_S, R_S, R_P, and C_P are derived as:

$$Ls=\frac{gm_{11}\left(1+gm_9R_5\right)C_T}{gm_8gm_9gm_{10}\left(1+gm_{11}R_6\right)}\quad Rs=\frac{gm_7gm_{11}\left(1+gm_9R_7\right)}{gm_8gm_9gm_{10}\left(1+gm_{11}R_6\right)}$$

$$R_P=ro_9\left(1+gm_9R_5\right)\qquad C_P=\left(Cgs_8+\left(1+\frac{gm_8}{gm_7}\right)Cgd_8\right) \tag{2}$$

Also, the quality factor and resonance frequency of AI can be calculated as follows:

$$\frac{1}{Q}=\frac{1}{gm_7}\times\sqrt{\frac{gm_8gm_9gm_{10}\left(1+gm_{11}R_6\right)C_T}{gm_{11}\left(1+gm_9R_5\right)C_P}}$$

$$\omega_0=\sqrt{\frac{gm_8gm_9gm_{10}\left(1+gm_{11}R_6\right)}{gm_{11}\left(1+gm_9R_5\right)C_T\left(Cgs_8+\left(1+\frac{gm_8}{gm_7}\right)Cgd_8\right)}} \tag{3}$$

The main part of AI circuit noise enters through the M9 current. By degenerating this transistor; in addition to increasing its impedance; it also reduces its current, which, as a result, reduces its noise level. Therefore, using the R5 reduces the injected noise by AI to LNA.

2-2- Input Impedance Analysis

According to Fig. 4, the input impedance of the LNA can be expressed as Eq. (4):

$$Zin=\left(\frac{1}{\left(gm_2+j\omega Cgs_2\right)\left(1+gm_1R_1\right)}\middle\|\frac{1}{\left(j\omega Cp_1\right)}\right) \tag{4}$$

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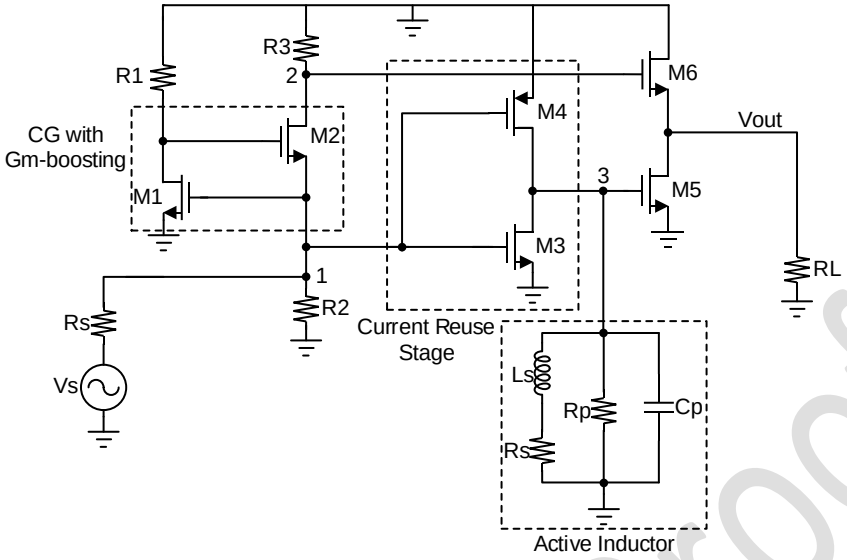

Fig. 4. The proposed circuit with AI

where Cp_1 is the parasitic capacitor of the input node and is expressed approximately as:

$$C_{P1} = Cgs_1 + Cgs_3 + Cgs_4 + Csb_2 + \left(1 + gm_1 R_1\right) Cgd_1 + \left(1 + \left(gm_3 + gm_4\right)\left(R_P \parallel R_S\right)\left(Cgd_3 + Cgd_4\right)\right) \quad (5)$$

As shown in Eq. (4), the input impedance depends on the transconductances of M1 and M2 and the sizes of M3 and M4. On the other hand, the size and DC bias point of transistors affect their generated noise, as explained next. Therefore, a trade-off exists between wideband input impedance matching and noise figure.

2-3- Gain Analysis

Assuming a complete matching in input and output in low frequency, we will have the following equations:

$$R_S = \frac{1}{\left(1 + gm_1 R_1\right) gm_2} \approx \frac{1}{gm_1 gm_2 R_1} \quad (6)$$

$$RL \approx \frac{1}{gm_6} \quad (7)$$

Substituting Eq. (6) and Eq. (7) in gain equation of the proposed circuit leads to Eq. (8).

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$$\frac{V_{OUT}}{V_S} = \left(gm_3 + gm_4\right) Z_{OUT1} \times \left(\frac{gm_5 RL}{2}\right) + \left(\frac{R_3}{2R_S}\right) \tag{8}$$

Where $Zout_1$ is the impedance at point 3 (refer to Fig. 4) and can be calculated as follows:

$$Zout_1 = \left(ro_3 \| ro_4\right) \| \left(Z_{AI}\right) \| \left(\frac{1}{j\omega Cp_3}\right) \tag{9}$$

where Cp_3 is the parasitic capacitor at node 3 in Fig. 4 and approximately equals to:

$$C_{p3} = Cgs_5 + \left(1 + \frac{gm_5 RL}{2}\right) Cgd_5 + Cgd_3 + Cgd_4 + Cdb_3 + Cdb_4 \tag{10}$$

Without AI, node 3 determines the dominant pole of the LNA because the parasitic capacitance and resistance in this node are high. Thus, the shunt peaking technique in this node can enhance the total bandwidth, as shown in the next section.

2-4- Noise Analysis

2-4-1 Active Inductor Noise

The noise sources of AI circuit are shown in Fig. 5.

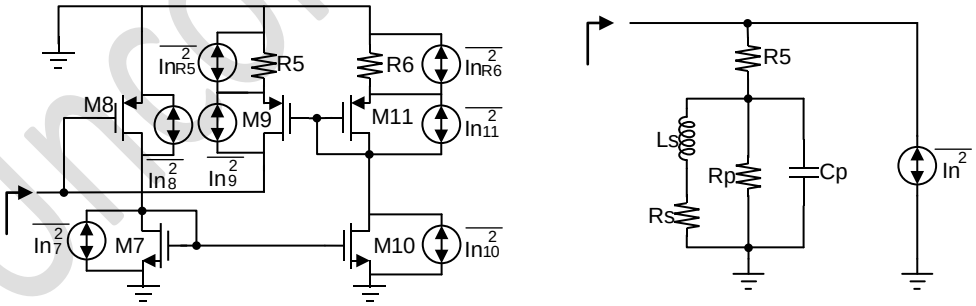

Fig. 5. The noise sources of AI and its equivalent circuit

The injected noise of AI is

$$\overline{InAI^2} = \left(\overline{InM_7{}^2} + \overline{InM_8{}^2}\right) \cdot \alpha_1{}^2 + \overline{InM_9{}^2} \cdot \alpha_2{}^2 + \overline{InM_{10}{}^2} \cdot \alpha_3{}^2 + \overline{InM_{11}{}^2} \cdot \alpha_4{}^2 + \overline{InR_5{}^2} \cdot \alpha_5{}^2 + \overline{InR_6{}^2} \cdot \alpha_6{}^2 \tag{11}$$

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Where α_1 to α_6 are defined as follows:

$$\alpha_1 = \left(\frac{gm_9 gm_{10} \left(\frac{1}{S_{Cx} + gm_7} \right) \left(gm_{11} ro_{11} R_6 \right)}{\left(1 + gm_{11} ro_{11} \right) \left(1 + gm_9 R_5 \right) + \left(gm_8 gm_9 gm_{10} \left(\frac{1}{S_{Cx} + gm_7} \right) Zout \right) \left(gm_{11} ro_{11} R_6 \right)} \right) \tag{12}$$

$$\alpha_2 = \left(\frac{\left(1 + gm_{11} ro_{11} \right)}{\left(1 + gm_{11} ro_{11} \right) \left(1 + gm_9 R_5 \right) + \left(gm_8 gm_9 gm_{10} \left(\frac{1}{S_{Cx} + gm_7} \right) Zout \right) \left(gm_{11} ro_{11} R_6 \right)} \right) \tag{13}$$

$$\alpha_3 = \left(\frac{gm_9 \left(gm_{11} ro_{11} R_6 \right)}{\left(1 + gm_{11} ro_{11} \right) + \left(gm_8 gm_9 gm_{10} \left(\frac{1}{S_{Cx} + gm_7} \right) Zout \right) \left(gm_{11} ro_{11} R_6 \right)} \right) \tag{14}$$

$$\alpha_4 = \left(\frac{gm_9}{\left(1 + gm_9 R_5 \right) \left(gm_{11} \right) + \left(gm_8 gm_9 gm_{10} \left(\frac{1}{S_{Cx} + gm_7} \right) Zout \right) \left(1 + gm_{11} R_6 \right)} \right) \tag{15}$$

$$\alpha_5 = \left(\frac{gm_{11} R_5}{\left(1 + gm_8 gm_{10} \frac{1}{S_{Cx} + gm_7} Zout \left(1 + gm_{11} R_6 \right) + gm_{11} R_5 \right)} \right) \tag{16}$$

$$\alpha_6 = \left(\frac{gm_9 gm_{11}{}^2 R_6 \left(\frac{1}{S_{Cx} + gm_7} \right)^2}{\left(1 + gm_9 R_5 \right) \left(gm_{11} \left(\frac{1}{S_{Cx} + gm_7} \right) \right) + \left(gm_8 gm_9 gm_{10} Zout \right) \left(1 + gm_{11} R_6 \right)} \right) \approx \left(\frac{gm_9 gm_{11} R_6}{\left(1 + gm_9 R_5 \right) \left(\frac{1}{S_{Cx} + gm_7} \right)} \right) \tag{17}$$

The noise generated by M1, M2, and R1 is depicted in Fig. 6. As shown in the figure, the noise appears in nodes 1 and 2 with opposite polarities. Thus, the noise components related to the first stage can be canceled using the "cancelling technique". Assuming perfect matching in the output, the condition of Eq. (18) must be met to cancel the noise of M2:

$$\left(gm_3 + gm_4 \right) = \frac{R_3}{2 gm_5 ZoutRsR_L} \tag{18}$$

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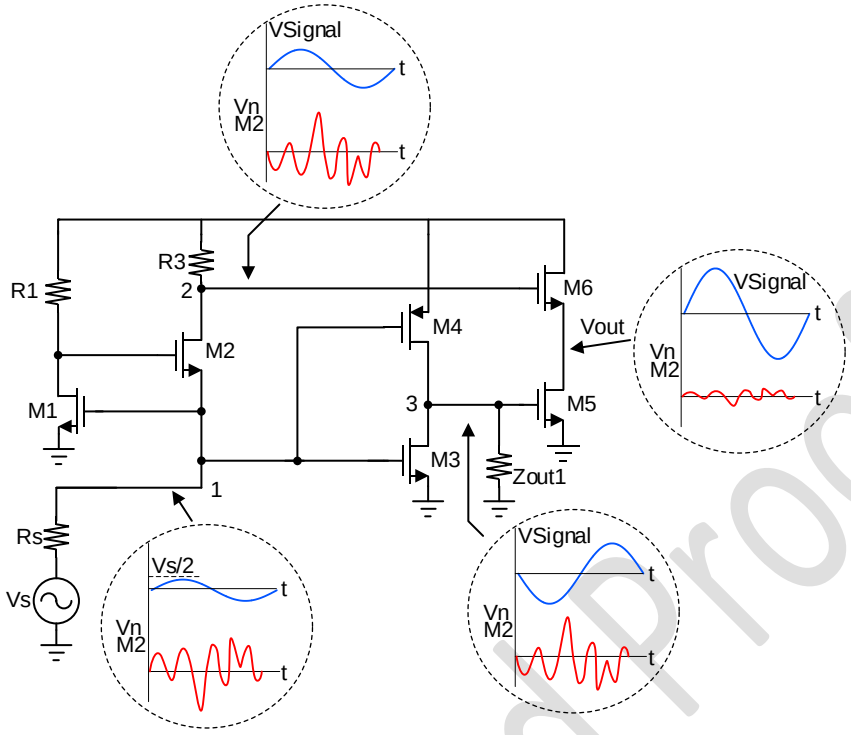

Fig. 6. The mechanism of canceling the noise of M2

2-5- Linearity Analysis

It is clear that the last stage is the dominant linearity contributor of the amplifier; thus, in the proposed circuit, M_5 and M_6 significantly affect the total linearity. The simulation results in [8] showed that combining the amplified input signal in two paths (using common source and common gate stages) can improve nonlinearity. In this section, using the proposed method in [8], we will examine how to improve the linearity of the circuit. In this work, we obtain the nonlinearity coefficients by taking derivatives of the DC relationship between *Vo* and *Vi* (refer to Eq. (19)) [2] and then verify it by simulations using Spectre-RF software:

$$\alpha_1 = \frac{\partial Vo}{\partial Vi} \qquad \alpha_2 = \frac{1}{2!}\frac{\partial^2 Vo}{\partial Vi^2} \qquad \alpha_3 = \frac{1}{3!}\frac{\partial^3 Vo}{\partial Vi^3} \tag{19}$$

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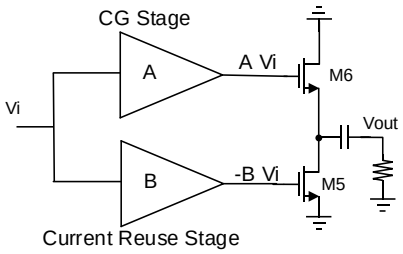

Fig. 7. CG and CS paths of the proposed LNA

As depicted in Fig. 7, the outputs of the two stages are combined by using M_5 and M_6 to form *Vout*. To simplify, all transistors are assumed to be in the saturation region. After derivation of *Vout* versus *Vin*, AIP_3 can be expressed as:

$$AIP3 = \sqrt{\frac{2X \cdot Y^4}{K_6 R_L \left[2(AY - X) + AY\right]\left[R_L\left(-K_6 (AY - X)^3 + Y^2 \left(K_5 \cdot B^2\right)\right)\right]}} \tag{20}$$

where *X* and *Y* are given by Eq. (21) and *A* and *B* are the gain of amplifiers in Fig. 7.

$$\begin{aligned} X &= R_L \left(gm_5 \cdot B + gm_6 \cdot A\right) \\ Y &= \left(1 + gm_6 R_L\right) \end{aligned} \tag{21}$$

To maximize the *AIP3*, the following condition is necessary.

$$A = \frac{2R_L \left(gm_5 \cdot B\right)}{\left(3 + gm_6 R_L\right)} \tag{22}$$

The trade-off between the NF and linearity for LNA circuit design should be carefully considered.

3- Simulation Result

The proposed circuit is simulated in 130 nm CMOS technology using Cadence Spectre-RF. The post-layout simulation is performed from 0.1 to 5 GHz. Package effects such as produced inductors by wire bonds and appeared capacitors by ESD pad are also considered, which has been shown in Fig. 8. According to Eq. (2), to investigate AI effect, S21 is simulated by several AI values, as shown in Fig. 9. According to Fig. 9, the bandwidth is limited without using *Cx* (AI and Shunt Inductive peaking) and with the proper selection of *Cx*, the bandwidth of the proposed LNA has reached 3.75 GHz.

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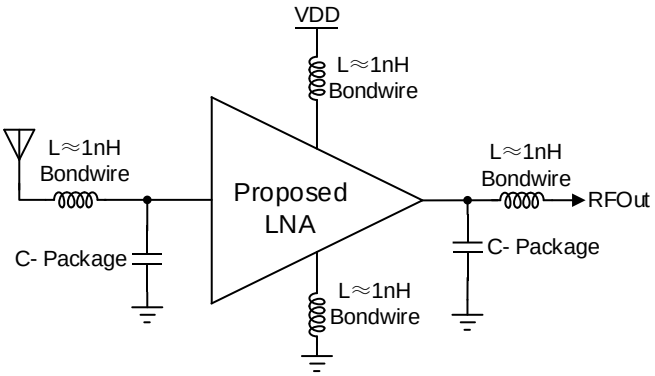

Fig. 8. Effects of wire bonds and capacitors created in the proposed LNA

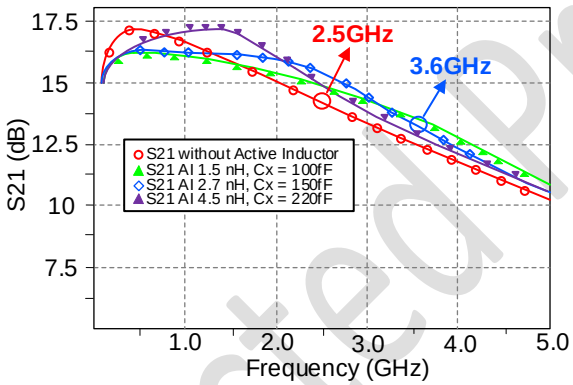

Fig. 9. Power gain curve and -3dB bandwidth for different values

Fig. 10 depicts the input and output reflections and shows that S_{11} and S_{22} remain below -15 dB from 0.25 GHz to 3.75 GHz. Output matching is necessary because the output must be connected to the next stage through the transmission line. The noise figure and power gain of the proposed circuit in two types of schematics and post-layout simulation are shown in Fig. 11, in which the highest gain is equal to 15.5 dB, and also the noise figure of the circuit for the frequencies of 0.5 GHz to 3.75 GHz is below 2.5 dB. The average value of the noise figure is equal to 2.3 dB, which is better than [8] , [14] and [15]. The bandwidth of the proposed circuit is equal to 3.5 GHz, which is very suitable for broadband applications. To simulate the linearity of the circuit, the two-tone test method is used, and two signals with a frequency difference of 10 MHz and frequencies of 1.99 GHz and 2 GHz are applied to the input. The results of this simulation have obtained the numbers -16.5 dBm and -5.5 dBm for P_{1DB} and IIP_3, respectively, which are plotted in

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Fig. 13. Also, the power consumption of the proposed circuit is equal to 4.7 mW from a 1V source. To ensure the stability of the circuit, the Rollet stability factor (Kf) is plotted in Fig. 14. As shown in the figure, the Kf is more than 10 for all frequencies, which shows the LNA is unconditionally stable. The combination of CG stage and CS stage not only increases the power gain but also improves the NF and input impedance matching. Fig. 15 shows the changes of the important parameters of the circuit in different corners compared to the normal TT mode at 2 GHz frequency. According to this diagram, parameter S_{11} is the most sensitive parameter. However, in the worst case, it is equal to -15 dB, which is an acceptable value. In the SS corner, the gain has decreased due to the low power consumption, and the noise figure has increased, while the opposite has happened in the FF mode. Fig. 16 illustrates the proposed circuit layout, whose occupied area is equal to 0.047mm^2. Simulation has also been done in different corners, and Table 1 compares the results at TT@27°C and the other cases, namely SS@80°C, FF@-20°C, FS@-20°C, SF@-20°C, FS@80°C and SF@80°C. According to the results of this table, the parameters are acceptable even in the worst case. The values of the elements used in AI are shown in Table 2. Table 3 compares all the results obtained with those of several similar works. The FOM is also included in the table and defined in Eq. (23) to compare our design quantitatively with other designs [8].

$$FOM = 20log_{10}\left(\frac{IIP3[mW]G_{av}[lin]Bandwidth[GHz]}{P_{DC}[mW](F_{av}[lin]-1)}\right) \quad (23)$$

According to Table 3, the proposed circuit has a higher FOM. Some references [6, 16] have a better figure of merit, but it should also be considered that the impedance matching is not included in their output, as a result, the power consumption and also the gain of their circuit are highly optimized, which has increased their FOM. Although [17] and [18] are better in some parameters, they lack impedance matching in the output.

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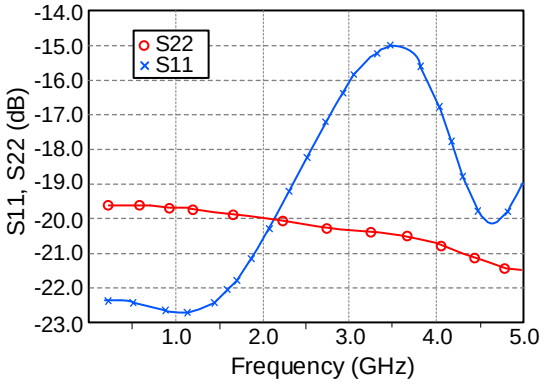

Fig. 10. Simulation results for input and output return losses

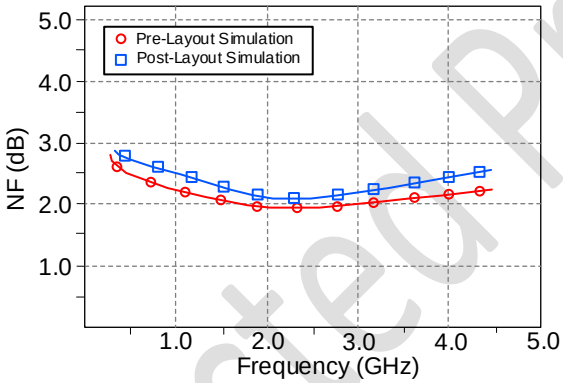

Fig. 11. Simulated noise figure in two schematic and post-layout simulation modes

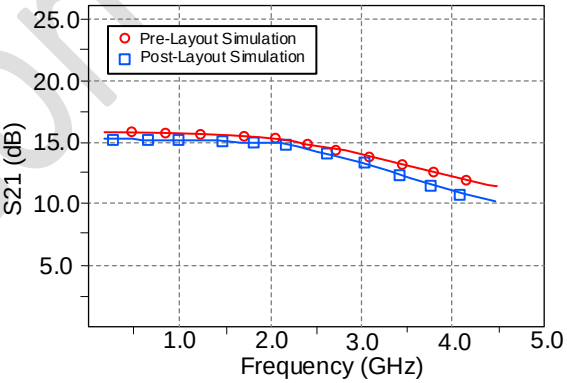

Fig. 12. Simulated S21 in two modes, schematic and post-layout simulation

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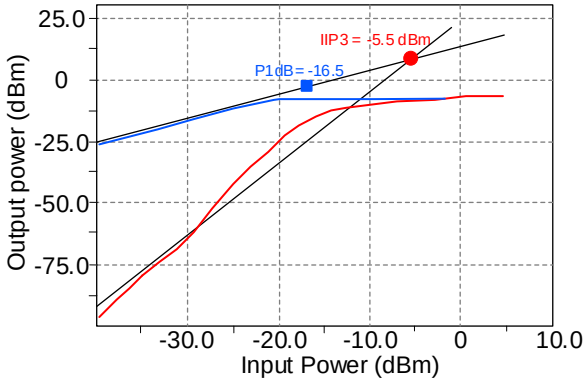

Fig. 13. Two-tone test at 2 GHz

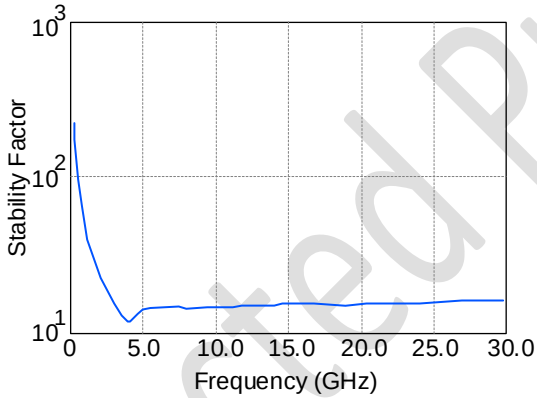

Fig. 14. Post-layout simulated of Rollett stability factor (Kf) of the proposed circuit

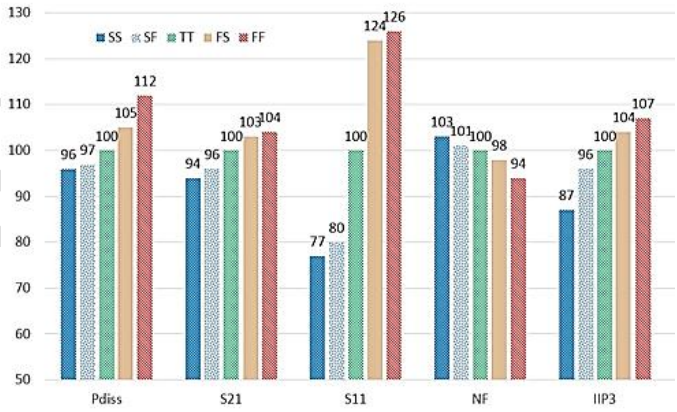

Fig. 15. Percentage changes of parameters at different corners, normalized to TT mode at 2 GHz.

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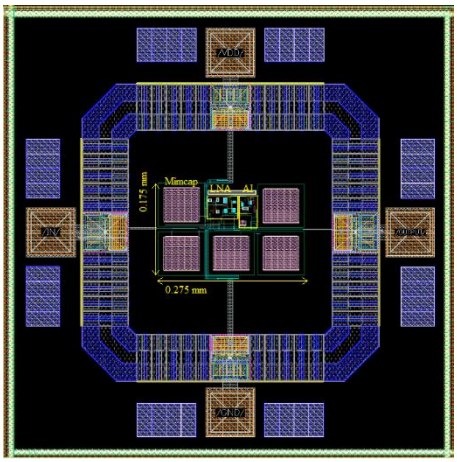

Fig. 16. The layout of proposed LNA

Table 1. Comparison between results at TT@27°C and other corners

Process Corners	TT@27°C	SS@80°C	FF@-20°C	SF@80°C	FS@80°C	SF@-20°C	FS@-20°C
P dis (mW)	4.77	4.6	5	5	5	5	5
S11 (dB)	<-15	<-13	<-18	<-14.6	<-15.3	<-15.6	<-16.35
S21 (dB)	15±1	14±0.2	16±0.3	14.3±0.2	14.5±0.3	15±0.25	15.5±0.3
NF (dB)	2.25±0.3	2.6±0.25	2±0.15	2.3±0.25	2.4±0.3	2.2±0.15	2.32±0.3
IIP3(dBm)	-5.5	-6.4	-5	-6.15	-6	-5.7	-5.4

Table 2. The values of the elements used in AI

Transistors W(µm) / L(µm)	Resistance (OHM)
M7 7 / 0.13	R5 380
M8 35 / 0.13	R6 380
M9, M11 20 / 0.13	
M10 10 / 0.13	

Table 3. Summary of simulation results with comparison with recent similar works

Reference	[8]	[9]	[19]	[6]	[16]	[17]	[18]	This Work
BW (GHz)	0.1-1.8	0.1-6.1	0.3-4.4	0.1-1.2	0.1-2.1	1.5-9.3	0.1-3.5	0.2-3.75
S11 (dB)	<-7.8	-11	<-10	<-10	<-10	<-11.6	<-7	<-15

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S21 (dB)	14.5	19	26.7	21.2	19.2	13.2	17	15±1
NF (dB)	3.0-3.8	2.3	3.0-3.5	2.6	2.4	2	2.6	2.25±0.3
IIP3 (dBm)	0.25	-16	-14.2	+6	+8.6	-4.6	+6.5	-5.5
Tech (nm)	180	180	65	130	130	65	65	130
PDiss (mw)	10.8	7.3	13.9	1.52	3.1	4.5	6.6	4.77
Inductor-less	YES	NO	YES	YES	YES	YES	YES	YES
Size (mm2)	0.055	0.7	0.009	0.007	0.005	0.008	0.0062	0.047
Output Matching	YES	YES	YES	NO	NO	NO	NO	YES
Simulation/Measurement results	Meas	Sim	Meas	Meas	Meas	Sim	Meas	Sim
FOM	4.87	7.41	-12	32.2	35.3	11.02	31	13.6

4- CONCLUSION

This paper presented a broadband low-noise amplifier with a bandwidth of 3.5 GHz. The proposed circuit using 130nm CMOS technology is first analyzed, and then the post-layout is simulated using Cadence RFSpectre software. In this paper, it has been shown that the simulation results have confirmed the theoretical results to an acceptable extent. The inductive shunt Peaking technique is the main technique used to increase the frequency bandwidth. The inductor used is AI, which saves a lot of space. Also, by using the current-reuse technique as well as noise cancellation technique, power consumption, and noise figure have been reduced to an acceptable level. The post-layout simulation in 130 nm CMOS technology shows that the proposed circuit has a bandwidth between 0.25 and 3.75 GHz, a gain of 16 dB, a noise figure less than 2.5 dB, and an IIP_3 of about -5.5 dBm. Also, the values of S_{11} and S_{22} were equal to -15 dB and -19 dB, respectively. The output of the proposed LNA should be connected to the next stage by a transmission line. Therefore, the output matching is necessary. The power consumption of the proposed circuit is equal to 4.7 mW from a 1-volt source. The occupied area of the circuit is only equal to 0.047 mm^2.

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