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Cascaded Multilevel Inverters with Reduced Structures Based on a Recently Proposed Basic Units: Implementing a 147-level Inverter

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ABSTRACT: A multilevel inverter is capable of generating high-quality stepwise pseudo-sinusoidal voltage with low THD , applicable to high-power and high-voltage systems. These types of topologies may require a large number of switches and power supplies. This leads to much cost, large size, and complicated control algorithms. Thus, newer topologies are being proposed to decrease the number of power electronic devices for a large number of levels in output voltage. Recently, a new multilevel inverter has been reported in the literature to reduce component count. Its structure requires a lower number of active switches as compared to the existing ones. The available literature presents a generalization of the topology with an especial asymmetrical sources ratio, but no investigations are made for other symmetrical or asymmetrical sources ratio with cascaded configurations. This study presents a comprehensive analysis of cascaded topologies with the proposed basic units. The topology is analysed for both symmetric and asymmetric DC source configurations. Also, two algorithms for asymmetric source configuration suitable for cascaded structures are proposed. Moreover, the design and simulation of a 147-level inverter are presented under an optimal number of DC sources and power switches. Furthermore, experimental validation is performed by implementing a laboratory prototype.

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1- Introduction

Multilevel inverters have been growing in various industrial applications as an efficient solution for high voltage/power DC–AC conversion. Several topologies can be found in the literature, e.g. [1-6], in order to overcome the increasing need for higher power supplies. Multilevel inverters have successfully made their way into the industry and therefore can be considered a mature and proven technology [3]. The main advantage of such inverters is their ability to synthesize waveforms with higher voltage levels, introducing a solution to increase the inverter operating voltage above the voltage limits of classical semiconductors [5]. Other advantages are the improved output voltage quality, switches stresses reduction, the smaller output filter size, and reduction in electromagnetic interference (EMI) [3]. The multilevel voltage source inverters have recently been applied to many medium or high power industrial applications such as renewable energies, motor drive systems, power quality, flexible AC transmission systems, high-voltage, direct current (HVDC) electric power transmission systems, and many other applications [1-6].

Compared to the conventional two-level inverters, a major disadvantage of multilevel structures is that as the number of output voltage levels increases, the number of required power electronic switches increases considerably such that it makes the overall system complex and costly. It in turn causes reduction in reliability and more complexity in fault detection and maintenance of the inverter. In practice, it would be critical to lower the number of components used in the inverter. Among the multilevel topologies, the cascaded ones have achieved more popularity because of their simple structure and the ease of extending to higher voltage levels [3]. Cascaded multilevel inverters synthesize a medium voltage output based on a series connection of power cells [7]. These inverters utilize several floating capacitors or DC voltage sources to generate the required output voltage levels. The structure of multilevel inverters may be symmetric or asymmetric. In the symmetric topologies, all DC sources are equal that makes a good modularity but they have a large number of components for a high number of output voltage levels. It cannot be seen modularity in asymmetric topologies but they have significantly lower number of components for any specific number of voltage levels [3]. In recent years, various topologies for multilevel inverters have been presented to increase the number of components with the aim of simplifying their structures [3], [8-10].

With regards to decreasing the number of components, recently a single-phase topology called packed U cell (PUC) is introduced in [10] for DC–AC conversion. This topology is composed of one DC source and a number of flying capacitors. A detailed operation study of a seven-level PUC inverter is given in [10] to show the advantages and the effectiveness of the proposed schemes. Although [10] presents a generalization of the PUC topology with an especial asymmetrical sources ratio, no investigations are made for the other asymmetrical or symmetrical sources ratio with cascaded configurations.

This paper presents a comprehensive analysis of cascaded topologies of the PUC. The topology is analysed for both

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symmetric and asymmetric source configurations. Then, they are compared with each other using the analytical description of each configuration in terms of different parameters versus the number of levels. These parameters are the number of switches, blocking voltages of the switches, etc. subject to the optimal number of DC sources. These detailed comparisons will lead to the cascaded asymmetric PUC with DC sources ratio1 (CAPUC1) structure that shows the best performance in terms of the above-mentioned parameters among all discussed structures. This selected inverter is fully designed, analysed, simulated, and implemented for a 147-level prototype. Experiments verify the analysis and simulations of the designed structure.

2- Packed U cell multilevel inverter (PUC)

The introduced topology in [10] is composed of one DC source and a number of flying capacitors. The PUC can be classified as a combination between the flying capacitor (FC) and the cascaded H-bridges (CHB) topologies. This topology can be seen as asymmetric flying capacitors [10]. Each U cell consists of two power switches and one capacitor or DC source as shown in Fig. 1(a). A typical seven-level configuration for such structure is shown in Fig. 1 (b). It consists of one DC source, one capacitor, and six switches. Moreover, the number of voltage levels depends on the value of the voltage across the capacitors. In order to obtain seven levels, the second capacitor voltage in Fig. 1(b) must be regulated to yield 1/3 V_{dc} [10]. In this case, the output voltage is obtained from the following seven levels ($-V_{dc}$, $-2/3V_{dc}$, $-1/3V_{dc}$,0,$1/3V_{dc}$,$2/3V_{dc}$,V_{dc}). When using one DC source and three capacitors as shown in Fig. 1(c), the number of voltage levels will be 31. In this case, only ten power switches are required. In general, the numbers of the voltage levels and switches of the PUC topology rare obtained by

$$\begin{cases} N_{level} = 2^{N_{dc}+1} - 1 \\ N_{switch} = 2N_{dc} + 2 \end{cases} \quad (1)$$

where N_{dc} is the total number of capacitors and DC source. A relationship can be developed between N_{switch} and N_{level} by omitting N_{dc} from the two equations in (1), and it is given by

$$N_{level} = 2^{\frac{N_{switch}}{2}} - 1 \quad (2)$$

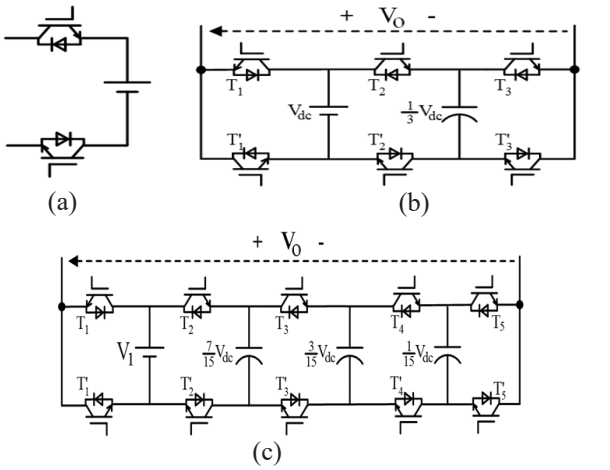


Fig. 1. Packed U Cell Multilevel Inverter Schemes, (a) Single U Cell (b) Single-Phase Seven-Level Inverter (c) Single-Phase 31-Level Inverter.

2- 1- Symmetric/ asymmetric PUCs

Consider generalized single-phase structure of packed U cell topology with only one DC sources and n-1 flying capacitors. By replacing all capacitors with DC sources, the configuration shown in Fig. 2(a) is obtained that has n number of input DC sources, which can be symmetrical or asymmetrical. It is clear this structure with symmetric DC sources can produce only three voltage levels that are not considered. With asymmetric DC sources ratio like (3), this inverter can produce $2^{n+1}-1$ different voltage levels at output according to (1). The authors call this structure as asymmetric paced U cell1 (APUC1).

$$V_i = (2^n - 1)V_{dc} \quad (3)$$

Another structure that can be assumed for the modified PUC is demonstrated in Fig. 2(b) in which the polarities of DC sources in Fig. 2 (a) are changed. This configuration is proposed in [8] with symmetric DC sources as structure A4 that can produce 2n+1 voltage levels in output. This structure is named symmetric packed U cell (SPUC) in this paper. The asymmetric configuration of the structure shown in Fig. 2(b) can be considered with DC source ratio like (4) that is named APUC2 in this study. The APUC2 with n DC sources can produce 4n-1 voltage levels that are higher than the ones produced by the SPUC.

$$\begin{cases} V_1 = V_{dc} \\ V_2 = 2V_1 = 2V_{dc}, \quad i = 2,3,\ldots,n \\ V_i = V_2 = 2V_{dc} \end{cases} \quad (4)$$

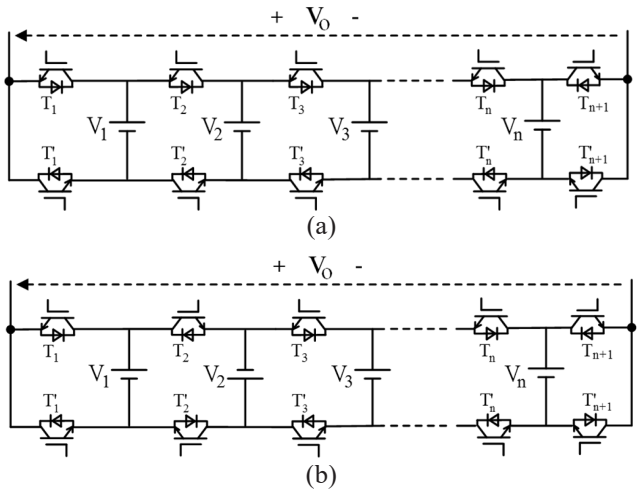


Fig. 2. Modified packed U cell structures examples, (a) asymmetric PUC (APUC1) (b) symmetric and asymmetric PUC (SPUC/ APUC2).

2- 2- Output Voltage

Let us consider a switching function S(t) for a given switch T as

$$S(t) = \begin{cases} 0, \textit{ switch T is blocking} \\ 1, \textit{ switch T is conducting} \end{cases} \quad (5)$$

Then, the output voltage for multilevel inverters shown in Fig. 2 can be expressed as

$$V_o(t) = \sum_{i=1}^{n+1} \left[(-1)^i (1 - S_i) V_{sw,i} \right] \quad (6)$$

where $V_{sw,i}$ is the blocking voltage of switch pairs (T_i,T_i') that can be obtained as it follows.

$$V_{sw,i}=\begin{cases} V_i - V_{i-1} \quad APUC1\left[Fig.2(a)\right] \\ V_i + V_{i-1} \quad APUC2 \text{ and } SPUC \left[Fig.2(b)\right] \end{cases} \tag{7}$$

Equation (6) can be rewritten by the following in terms of switching functions and the DC sources values.

$$V_o(t)=\sum_{i=1}^{n+1}\left[\left(S_i(t)-S_{i+1}(t)\right)V_{sw,i}\right] \tag{8}$$

For both structures shown in Fig. 2, the blocking voltage of switch pairs (T_1,T_1`) and ($T_{n+1}$,$T`_{n+1}$) is equal to V_1 and V_n, respectively, whereas for all the remaining switches the voltage stress $V_{sw,i}$ {i = 2, 3,…, n} can be obtained from (7). Also, the maximum voltage blocking in APUC1 related to T_{n+1} and $T`_{n+1}$ is V_n whereas $V_{sw,max}$ for the structure shown in Fig. 2(b) is V_n+V_{n-1}.

3- Cascaded packed U cell multilevel inverters (CPUCs)

To extend higher voltage levels in the multilevel inverter, cascaded configurations can be considered. This section cascading m basic units of PUCs (see Fig. 2) as shown in Fig. 3 compares these structures in order to obtain the required number of DC sources, the number of switches, the number of output voltage levels, stresses on the switches and other parameters.

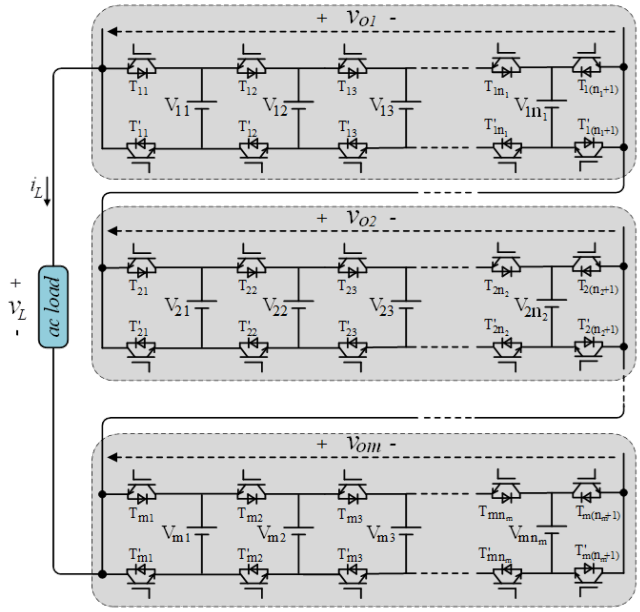


Fig. 3. Cascaded multilevel inverter using m basic unit of PUC structures.

3- 1- Cascaded asymmetric PUC1 (CAPUC1)

Assume Fig. 3 in which m cascaded APUC1 (see Fig. 2(a)) is presented; also, the number of identical DC sources within m basic modules are {n_1,n_2,…,n_m}. Let us further assume that n1 DC sources from the first module are according to (9). Then, the first module is capable of generating 2^{n_1+1}-1 output voltage levels according to (1).

$$\begin{cases} V_{11}=V_{dc} \\ V_{1i}=2V_{1(i-1)}+1=(2^i-1)V_{dc} \end{cases},\quad i=2,3,\ldots,n_1 \tag{9}$$

Hence, the second module is asymmetrical with respect to the first one to have a multilevel inverter with a maximum number of voltage levels (not to have redundant states). Therefore, this can be generalized for further modules to obtain a general definition for all DC sources within the kth module (k ≥ 2) by

$$\begin{cases} V_{k1}=2\sum_{i=1}^{k-1}V_{in}+1=\prod_{i=1}^{k-1}\left(2^{n_i+1}-1\right)V_{dc} \\ V_{ki}=\left(2^i-1\right)V_{k1} \quad , \quad i=2,3,\ldots,n_k \end{cases}. \tag{10}$$

Thus, using the suggested DC sources in (9) - (10), the maximum conceivable output voltage $V_{peakand}$ the total number of achievable levels N_{level} are

$$\begin{cases} V_{peak}=V_{1n_1}+V_{2n_2}+\ldots+V_{mn_m}=\sum_{k=1}^{m}V_{kn_k} \\ N_{level}=\prod_{k=1}^{m}\left(2^{n_k+1}-1\right) \end{cases} \tag{11}$$

Also, the total number of DC sources, say N_{dc}, and the total number of switches, say N_{switch}, for m modules are

$$\begin{cases} N_{dc}=n_1+n_2+\ldots+n_m=\sum_{k=1}^{m}n_i \\ N_{switch}=\sum_{k=1}^{m}\left[2n_k+2\right]=\sum_{k=1}^{m}2\left(n_k+1\right) \end{cases} \tag{12}$$

The maximum possible voltage stress on switches in a typical kth cascaded module ($V_{\_sw,k}$) with n_k DC sources in asymmetric condition can be calculated by

$$\begin{aligned} V_{sw,k}&=2V_{k,1}+2\left(V_{k,2}-V_{k,1}\right)+2\left(V_{k,3}-V_{k,2}\right) \\ &+\ldots+2\left(V_{k,n_k}+V_{k,n_k-1}\right)+2V_{k,n_k}=4V_{k,n_k} \end{aligned} \tag{13}$$

With considering m cascaded basic unit and using (11) and (13), the following equation for the total voltage stresses (V_{SW}) can be concerned.

$$\begin{aligned} V_{SW}&=V_{sw,1}+V_{sw,2}+\ldots+V_{sw,m}=\sum_{k=1}^{m}V_{sw,k} \\ &=\sum_{k=1}^{m}4V_{k,n_k}=4V_{peak}=2\left(N_{level}-1\right)V_{dc} \end{aligned} \tag{14}$$

With taking Vdc as the base value, per-unit value of total standing voltage ($V_{SW,pu}$) is attained by

$$V_{SW,pu}=\frac{V_{SW}}{V_{dc}}=2\left(N_{level}-1\right) \tag{15}$$

Also, the maximum blocking voltage on switches that is related to the mth module ($V_{sw,max}$) is V_{m,n_m}.

Assume it is desired to maximize N_{level} in (11) subject to fixed N_{dc} or N_{switch} in (12). It is clear that the product of the numbers, whose summation is constant, will be maximized when all the numbers are identical. Then, N_{level} is maximized when the number of DC sources in all modules are identical (n_1=n_2=...=n_m=n). Hence, applying this consideration in (11) and (12) results in:

$$\begin{cases} N_{dc} = mn \\ N_{\text{switch}} = 2m\left(n+1\right) \\ N_{\text{level}} = \left(2^{n+1}-1\right)^{m} \end{cases} \tag{16}$$

A relationship can be developed between N_{level}, N_{switch} and N_{dc} by omitting m from the three relations in (16).

$$N_{\text{level}} = \begin{cases} [\left(2^{n+1}-1\right)^{\frac{1}{2(n+1)}}]^{N_{\text{switch}}} \\ [\left(2^{n+1}-1\right)^{\frac{1}{n}}]^{N_{\text{dc}}} \end{cases} \tag{17}$$

Consider (17). To maximize N_{level} for a constant number of switches, the term $(2^{n+1}-1)^{1/(2n+2)}$ should be maximum. This term as can be seen in Fig. 4(a) has not a maximum point but for n≥6 has a very small variation. Also, to maximize N_level for a constant number of DC sources, the term $(2^{n+1}-1)^{1/n}$ should be maximized (n=1). With n=1, the discussed structure is converted to the conventional cascaded multilevel inverter (CHB). Thus, it is important to consider two DC sources in each module to apply the CAPUC1 with a maximum voltage level for the comparison. The number of required switches is relevant to the number of DC sources, thus if N_{dc} is optimum for achieving the maximum number of voltage levels, N_{switch} will also become optimum. Therefore, the CAPUC1 consisting of two DC sources in each module using minimum numbers of DC sources and switches can provide the maximum voltage levels.

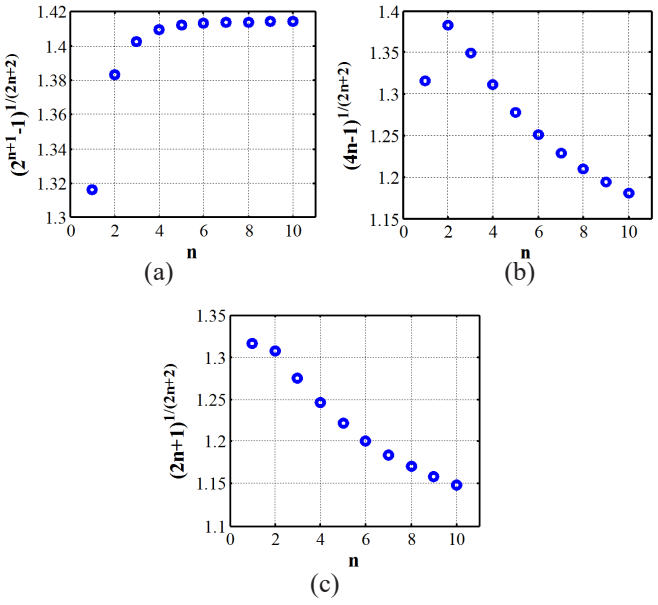


Fig. 4. Variation of (a) $(2^{n+1}-1)^{1/(2n+2)}$, (b) $(4n-1)^{1/(2n+2)}$ and (c) $(2n+1)^{1/(2n+2)}$ versus n.

3- 2- Cascaded asymmetric PUC2 (CAPUC2)

Assume m cascaded APUC2 shown in Fig. 2(b) with asymmetric DC sources according to (18) for the first module.

$$\begin{cases} V_{11} = V_{dc} \\ V_{12} = 2V_{11} = 2V_{dc}, \quad i = 2,3,\ldots, n_1 \\ V_{1i} = V_{12} = 2V_{dc} \end{cases} \tag{18}$$

To remove redundant states with the maximum number of voltage levels, the dc voltage sources of the second module must be asymmetrical with respect to the first one as follows:

$$\begin{cases} V_{21} = 2\sum_{k=1}^{n_1} V_{1k} + 1 = \left(4n_1 - 1\right)V_{dc} \\ V_{2i} = 2V_{21} = 2\left(4n_1 - 1\right)V_{dc} \\ i = 2,3,\ldots, n_2 \end{cases} \tag{19}$$

Also, the voltages of DC sources within the kth module are obtained as it follows.

$$\begin{cases} V_{k1} = 2\sum_{i=1}^{k-1}\sum_{j=1}^{n_i} V_{ij} + 1 = \prod_{i=1}^{k-1}\left(4n_i - 1\right)V_{dc} \\ V_{ki} = 2V_{k1}, \quad i = 2,3,\ldots, n_k \\ k = 2,3,\ldots, m \end{cases} \tag{20}$$

Thus, using the mentioned values of the dc voltage sources, one can calculate the maximum conceivable output voltage V_{peak} and the total number of achievable levels N_{level} by:

$$\begin{cases} V_{peak} = \sum_{k=1}^{m}\sum_{i=1}^{n_k} V_{ki} \\ N_{\text{level}} = 2\sum_{k=1}^{m}\sum_{i=1}^{n_k} V_{ki} + 1 = \prod_{k=1}^{m}\left(4n_k - 1\right) \end{cases} \tag{21}$$

The maximum possible voltage stress on switches in kth module ($V_{sw,k}$) with n_k DC sources can be obtained as it follows:

$$\begin{aligned} V_{sw,k} &= 2V_{k,1} + 2\left(V_{k,1} + V_{k,2}\right) + 2\left(V_{k,2} + V_{k,3}\right) \\ &+ \ldots + 2\left(V_{k,n_k-1} + V_{k,n_k}\right) + 2V_{k,n_k} = 4\sum_{i=1}^{n_k} V_{k,i} \end{aligned} \tag{22}$$

From (20), (21), and (22) and by considering m cascaded basic unit, the following equation for the total voltage stresses (V_{SW}) is developed.

$$\begin{aligned} V_{SW} &= \sum_{k=1}^{m} V_{sw,k} = 4\sum_{k=1}^{m}\sum_{i=1}^{n_k} V_{k,i} = \\ 4V_{peak} &= 2(N_{level} - 1)V_{dc} \end{aligned} \tag{23}$$

The per-unit value of total standing voltage ($V_{SW,pu}$) is calculated by

$$V_{SW,pu} = \frac{V_{SW}}{V_{dc}} = 2(N_{level} - 1) \tag{24}$$

Furthermore, the maximum blocking voltage on switches relevant to the mth module ($V_{SW,max}$) is $V_{m,n-1}+V_{m,n}$. Like the CAPUC1, the total number of DC sources and the total number of switches for m modules are equal to that stated by (12). Assume it is desired to maximize N_{level} in (21) subject to a fixed N_{dc} or N_{switch} in (12). Then, N_{level} is maximized when the number of DC sources in all modules are identical. Hence, applying this fact to (12) and (21) results in:

$$\begin{cases} N_{dc} = mn \\ N_{switch} = 2m\left(n+1\right) \\ N_{level} = \left(4n-1\right)^{m} \end{cases} \quad (25)$$

A relationship can be developed between N_{level}, N_{switch}, and N_{dc} by omitting m from the three equations in (25).

$$N_{level} = \begin{cases} [\left(4n-1\right)^{\frac{1}{2(n+1)}}]^{N_{switch}} \\ [\left(4n-1\right)^{\frac{1}{n}}]^{N_{dc}} \end{cases} \quad (26)$$

From (26) and Fig. 4(b) it can be inferred that N_{level} is maximum for a constant number of switches with n=2. Also, for a constant DC source number, N_{level} is maximum when n=1. Thus, to apply the CAPUC2 with maximum voltage level by using minimum numbers of switches and DC sources, two DC sources in each module should be considered.

3- 3- Cascaded symmetric PUC (CSPUC)

Assume m cascaded SPUC (see Fig. 2(b)) with n1 DC sources equal to V_{dc} in the first module (symmetric DC sources), then the first module is capable of generating $2n_1+1$ output voltage levels. To have more voltage levels, the second module is asymmetrical with respect to the first one. Therefore, this can be generalized for further modules to obtain the voltages of DC sources within the kth module ($k \geq 2$) as it follows. Note that the DC sources have to be identical in each module.

$$\begin{cases} V_{11} = V_{12} = \ldots = V_{1n_1} = V_{dc} \quad , \; k \geq 2 \\ V_{k1} = V_{k2} = \ldots = V_{kn_k} = \prod_{i=1}^{k-1}\left(2n_i+1\right)V_{dc} \end{cases} \quad (27)$$

Consider (27). The maximum conceivable output voltage V_{peak} and the total number of voltage levels N_{level} are:

$$\begin{cases} V_{peak} = \sum_{k=1}^{m} n_k \times V_{k1} \\ N_{level} = 2\sum_{k=1}^{m}\sum_{i=1}^{n_k} V_{ki} + 1 = \prod_{k=1}^{m}\left(2n_k+1\right) \end{cases} . \quad (28)$$

It is notable that because of the same configuration in CSPUC and CAPUC2, the maximum possible voltage stress on switches in kth cascaded module ($V_{sw,k}$), the total voltage stresses for all switches (V_{SW}), and the per-unit value of total standing voltage ($V_{SW,pu}$) are obtained from (22), (23) and (24), respectively. Also the maximum blocking voltage on switches ($V_{SW,max}$) is $V_{m,n-1}+V_{m,n}$.

Like the two previous discussed structures, N_{level} in (28) subject to a fixed N_{dc} or N_{switch} is maximized when the number of DC sources in all modules are identical. Therefore, N_{level} can be rewritten as

$$N_{level} = \left(2n+1\right)^{m} \quad (29)$$

By omitting m from (29) and considering N_{switch} and N_{level} in (25), a relationship can be developed as (30). Considering (30) and Fig. 4(c) N_{level} is maximum with n=1 for a constant number of switches and n=2 for a constant number of DC source. Thus, to apply the CSPUC with maximum voltage level using minimum numbers of DC sources and switches, like the CAPUC1 and the CAPUC2, two DC sources in each module should be considered.

$$N_{level} = \begin{cases} [\left(2n+1\right)^{\frac{1}{2(n+1)}}]^{N_{switch}} \\ [\left(2n-1\right)^{\frac{1}{n}}]^{N_{dc}} \end{cases} \quad (30)$$

4- Analytical comparison of discussed structures

4- 1- Comparison and discussion

Different parameters for two asymmetric and one symmetric discussed cascaded multilevel inverter in the previous section based on conventional packed U cell structure are listed in Table I. These parameters are calculated for a different number of DC sources with a different available number of modules. Note that PUC in Table I is a conventional un-cascaded PUC (see Fig. 2(a)) with N_{dc} DC sources. All the four discussed multilevel inverters, including CSPUC, CAPUC1, CAPUC2 and PUC, are comparable in terms of various aspects discussed in the following

- With n=1 for all modules, all three cascaded structures in Table I are changed to CHB.
- With m=1 for any number of DC sources (n) the CAPUC1 is equivalent to conventional PUC.
- By considering two DC sources in each module (n=2), the CAPUC1 and CAPUC2 have the same parameters.
- For n≥3, the CAPUC1 is able to produce more voltage levels rather than other structures.
- With an equal number of DC sources in all or almost all modules, the maximum voltage levels are available.
- With a certain number of DC sources in each module (n), after using more modules (m), it is possible to generate more voltage level that it is maxzimized with n=2 for all modules.

4- 2- Selection of best structure

Comparing structures discussed in the previous section shows the following facts according to the foregoing discussions:

- if the aim is to maximize the number of voltage levels with a fixed number of switches or DC sources, as discussed in Section 3, using only two DC sources in each module (n=2), the CAPUC1 and CAPUC2 with the same parameters are the best choices.
- using more than two DC sources in each module, the CAPUC1 generates more voltage levels. Hence, this structure is the optimal one among all structures in terms of the lowest number of DC sources and switches.

Assume a given number of levels. By considering the above facts, the CAPUC1 can be utilized for applications that employ inverters with more elements in a cascaded configuration. This research will be continued by designing

and implementing CAPUC1 to confirm its capabilities for the discussed analysis and simulations.

5- Design of a single phase multilevel inverter based on CAPUC1

5- 1- Power circuit design

Given a given number of levels, the design of a single-phase inverter with the CAPUC1 is explained as the best structure. Assume $N_{level} \geq 140$ is desired, where the two sources are considered per module (optimal design with n=2). According to Table I, choosing m=2 results in Nlevel =49, and m=3 yields N_{level} =343. The both are rather far from the assumed region. Then, considering n=3 with m=2 results in N_{level} =225 that is also more than the required number of levels. Based on (11) and (12), considering n=2 as the optimal design would result in m=2.5 with 147 levels that are very close to our assumption. The module number m=2.5 denotes two modules with n=2 and one module with n=1. Therefore, the closest configuration to 140 levels would be three cascaded modules, where the two modules consist of two DC sources and another one has only one DC source (H.B). Fig. 5 shows the combination of such a selected set of parameters for the CAPUC1. Let us assume that the base value of DC sources in Fig. 5 (V_{dc}) be 1V. Identical maximum output voltage can be worked out using (12) as it follows.

$$v_{o-max} = V_{peak} = \sum_{k=1}^{3} V_{kn_k} = \left(V_{12} + V_{22} + V_{31}\right) = 3V_{dc} + 21V_{dc} + 49V_{dc} = 73V_{dc} = 73V \quad (31)$$

Then, DC sources voltages in the first module are 1 V and 3 V, while in the second module are 7 V and 21 V according to (10) and (11). Also, the DC source voltage in the third module (H.B) is 49V. The total breaking voltage is 292 V for all switches according to (14). Additionally, the maximum voltage stress, i.e. 49 V, drops on the switches of the third module.

5- 2- Switching states and control scheme

Different modulation techniques are available for multilevel inverters in order to follow a particular goal [11–12].

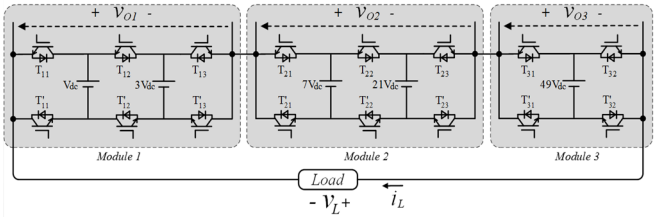


Fig. 5. A 147 -Level Single-Phase Multilevel Inverter Based on the CAPUC1 (two module with n=2 and one module with n=1 (m=2.5)).

The designed multilevel topology in the previous section can be modulated with popular strategies such as level-shifted sinusoidal pulse-width modulation (LS-SPWM) [3], selective harmonic elimination (SHE), etc. [11]. Another popular scheme is space-vector PWM [13] but it becomes very complicated for more than five levels and hence the scheme is not dealt in this paper. When the number of levels is high, the fundamental switching technique could be a useful modulation method [14]. One advantage of this technique is its low switching frequency in comparison with other techniques such as LS-PWM.

Various control schemes were introduced in the literature for

Table 1: Calculated parameters for the four discussed structures for a various number of dc sources and modules.

N_{dc}	n_1	n_2	n_3	m	structure	N_{level}	N_{switch}
2	2	×	×	1	CSPUC	5	6
					CAPUC1	7	
					CAPUC2	7	
	×	×	×	×	PUC	7	
3	3	×	×	1	CSPUC	7	8
					CAPUC1	15	
					CAPUC2	11	
	2	1	×	2	CSPUC	15	10
					CAPUC1	21	
					CAPUC2	21	
	×	×	×	×	PUC	15	8
4	4	×	×	1	CSPUC	9	10
					CAPUC1	31	
					CAPUC2	15	
	3	1	×	2	CSPUC	21	12
					CAPUC1	45	
					CAPUC2	33	
	2	2	×	2	CSPUC	25	12
					CAPUC1	49	
					CAPUC2	49	
	×	×	×	×	PUC	31	10
5	5	×	×	1	CSPUC	11	12
					CAPUC1	63	
					CAPUC2	19	
	4	1	×	2	CSPUC	27	14
					CAPUC1	93	
					CAPUC2	45	
	3	2	×	2	CSPUC	21	14
					CAPUC1	105	
					CAPUC2	33	
	2	2	1	3	CSPUC	75	16
					CAPUC1	147	
					CAPUC2	147	
	×	×	×	×	PUC	63	12
6	6	×	×	1	CSPUC	13	14
					CAPUC1	127	
					CAPUC2	23	
	5	1	×	2	CSPUC	33	16
					CAPUC1	189	
					CAPUC2	57	
	4	2	×	2	CSPUC	45	14
					CAPUC1	217	
					CAPUC2	105	
	3	3	×	2	CSPUC	47	16
					CAPUC1	225	
					CAPUC2	121	
	2	2	2	3	CSPUC	125	18
					CAPUC1	343	
					CAPUC2	343	
	×	×	×	×	PUC	127	14

Table 2: switching states for 147-level capuc1.

Switches states								
Module1			Module2			Module3		$\frac{v_o}{V_{dc}}$
T_{11}	T_{12}	T_{13}	T_{21}	T_{22}	T_{31}	T_{31}	T_{32}	
1	1	0	1	1	0	1	0	73
0	1	0	1	1	0	1	0	72
1	0	0	1	1	0	1	0	71
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	0	0	0	0	0	0	2
1	0	0	0	0	0	0	0	1
1	1	1	1	1	1	1	1	0
0	0	0	0	0	0	0	0	
0	1	1	1	1	1	1	1	-1
1	0	1	1	1	1	1	1	-2
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	0	0	1	0	1	-71
1	0	1	0	0	1	0	1	-72
0	0	1	0	0	1	0	1	-73

multilevel inverters [12], which are based on determining the desirable instantaneous voltage level for the output. Besides, the instantaneous voltage level is determined. Table II gives a lookup table for switching states of 147 different levels involved in the designed CAPUC1 structure (see Fig. 5) and gives those switches that have to be turned on. The implemented CAPUC1 was modulated with the fundamental technique in order to clarify the engaged technique. The 147-level inverter is controlled in an open-loop manner by applying a sinusoidal reference to build up the required instantaneous voltage level. In fact, the reference voltage is a 50 Hz sinusoidal voltage having a peak of 146 V that the implemented inverter has to generate it in 147 levels. The main objective is to create an output voltage with a slim difference from the desired reference.

6- SIMULATIONS AND EXPERIMENTS

This section begins with the introduction of simulations for the designed cascaded multilevel inverter; then, the implemented CAPUC1 is presented that verifies the performed analysis and simulations.

6- 1- Simulations

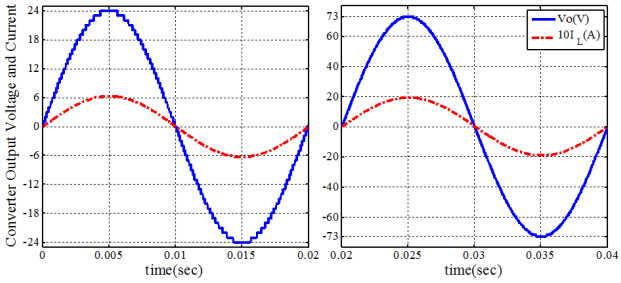
The CAPUC1 provides a high number of output levels if the number of DC voltage sources is increased. In other words, up to 147 levels will be available only if five DC voltage sources are employed in a single phase inverter (see Fig. 5). Hence, the designed 147-level CAPUC1 is simulated. The switches of the inverter are modulated based on the technique discussed in Section 5.2. The simulated output voltage and the current of the inverter are illustrated in Fig. 6. The reference voltage is changed from 48 V (peak-to-peak, 49 levels) in Fig. 6(a) to 146 V (peak-to-peak, 147 levels) in Fig 6(b) at t=0.02sec. The THD of the output voltage and the current in Fig. 6(b) are 0.55% and 0.16%, respectively, that are very close to a pure sinusoidal waveform due to the high number of levels. The current (multiplied by ten) is very smooth as shown in Fig. 6.

Figs. 7 depicts the behavior of the inverter modules, showing the voltage of each module as well as their aggregate voltage. It can be seen that the switching frequency of the first module is bigger than two other ones. The bigger the number of modules, the lower would be the switching frequencies of the right modules. In a medium/high voltage design, one can apply switches with low switching frequencies to the bottom modules in Fig. 3 (e.g. IGCT), and high switching frequency switches to the upper modules (e.g. IGBT). In fact, the major drawback of the IGCT technology is its limited switching frequency; whereas IGBT technology cannot sustain high power once operating at medium frequency [10].

6- 2- Experimental validation and analytical discussions

A laboratory prototype was implemented to validate the designed CAPUC1 (see section 5). The microprocessor EZDSP TMS320F28335 was used to implement the switching algorithm discussed in section 5.2. Five isolated low-power DC sources were engaged in supplying the required voltages of each module. Table III lists specifications of the designed CAPUC1.

Fig. 8 shows experiments for the load defined in Table III, including the RL-load voltage and the current for two voltage references, including 48 V (peak-to-peak, 49 levels) in Fig. 8(a) and 146 V (peak-to-peak, 147 levels) in Fig 8(b). The THD of voltage and the current waveforms in Fig. 8(b) are 1.63% and 0.72%, respectively.



(a) **(b)**

Fig. 6. Simulated Output Voltage and Current of 147-lLevel CAPUC1: (a) 48 V (peak-to-peak, 49 levels) (b) 146 V (peak-to-peak, 147 levels)

Table 3: specifications of the implemented 147-level capuc1.

No	Title		Specifications	Quantity
1	IGBT		BUP314,35A,1200V	16
2	IGBT Driver		TLP 250, ±30 V, 1 A	16
3	Microprocessor		EZDSP TMS320F28335	1
4	Switching Technique		Fundamental Frequency Switching	---
5	Power Supplies Voltage	Module1	V11=1 V, V12=3 V	2
		Module2	V21=7 V, V22=21 V	2
		Module3	V31=49 V	1
6	Load		RL(R=40Ω, L=2mH)	1
7	Fundamental Frequency		50Hz	---

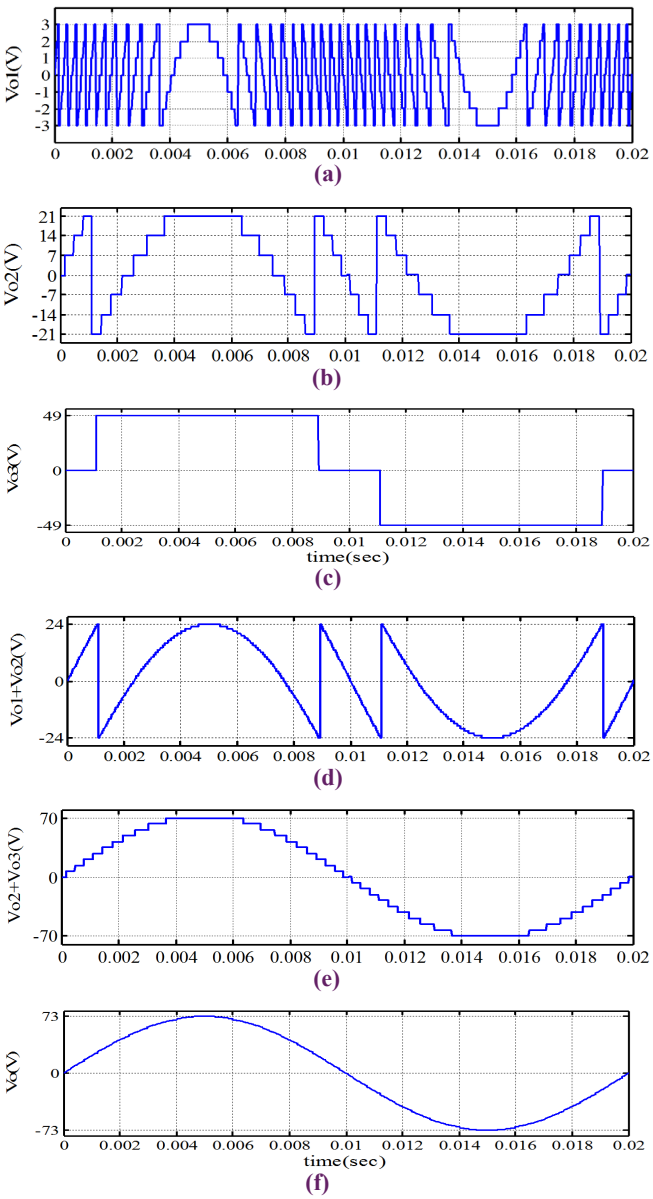


Fig. 7. Simulated output voltages of modules while the inverter generates 147 level at output voltage, (a) V_{o1} (b) V_{o2} (c) V_{o3} (d) $V_{o1}+V_{o2}$ (e) $V_{o2}+V_{o3}$ (f) $V_o=V_{o1}+V_{o2}+V_{o3}$

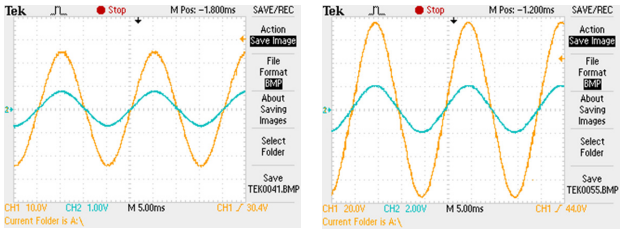


Fig. 8. Steady State Operation of the CAPUC1: Experimental Voltage and Current of Load, (a) 48 V (peak-to-peak, 49 levels) (Amp /div =1 A) (b) 146 V (peak-to-peak, 147 levels) (Amp /div =2 A).

Comparing experiments with those of simulations in Fig. 6 (a) confirms accurate output voltage build up, having a very close current waveforms along with a small difference in the THD due to practical imperfect parameters. Additionally, the output voltages of the three modules, as well as their aggregated voltages, are shown in Fig. 9.

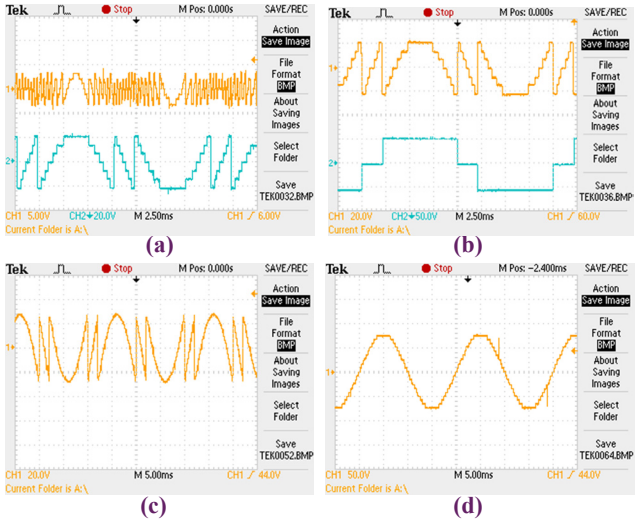


Fig. 9. Steady State Operation of the CAPUC1: Experimental Voltages of Modules for Producing 147 Levels at Output Voltage, (a) V_{o1} and V_{o2} (b) V_{o2} and V_{o3} (c) $V_{o1}+V_{o2}$ (d) $V_{o2}+V_{o3}$.

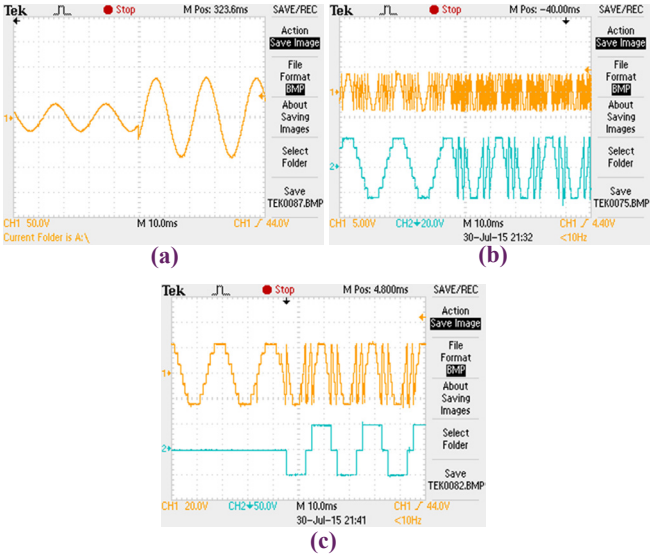


Fig. 10. Dynamic Behavior of 147-Level Inverter for Changing Reference Voltage from 48 V (peak-to-peak, 49 levels) to 146 V (peak-to-peak, 147 levels), (a) Inverter Output Voltage (b) V_{o1} and V_{o2} (c) V_{o2} and V_{o3}.

Furthermore, assume the reference voltage changes from 48 V (peak-to-peak, 49 levels) to 146 V (peak-to-peak, 147 levels). Experiments in Fig. 10 show the rapid rise of modules' voltages and the fast response in the dynamic behavior for tracking the voltage variations.

The structure CAPUC1 can be applied to various applications such as renewable energy conversion like photovoltaic systems, fuel cell, battery storage, etc. Also, the implemented 147-level topology can be used in single-phase UPS applications that create high quality sinusoidal AC output.

7- Conclusion

A detailed analysis of cascaded symmetrical and asymmetrical configurations based on newly proposed basic units (packed U cell) was presented in this paper. This study was based on the achievement of more voltage levels with a reduction in the number of power electronic components. The analyses show that by using only two DC sources in each cascaded

module (n=2), the CAPUC1 and CAPUC2 generate the maximum number of voltage levels with a fixed number of DC sources and switches. By exploiting more than two DC sources in each module, the CAPUC1 generates more voltage levels. Thus, the CAPUC1 has an optimal structure among all discussed structures. This reduced structure could be applied into inverters with a lower number of devices such as DC sources and switches. Further, a 147-level inverter was implemented based on the CAPUC1 structure. This inverter is capable of creating 147 levels with the lower number of devices compared to other discussed structures. The experiments and the simulations confirmed the validity of the discussions and analyses.

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